Effects of advanced process approaches on electromigration degradation of Cu on-chip interconnects

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Abstract

This thesis provides a methodology for the investigation of electromigration (EM) in Cu-based interconnects. An experimental framework based on *in-situ* scanning electron microscopy (SEM) investigations was developed for that purpose. It is capable to visualize the EM-induced void formation and evolution in multi-level test structures in real time. Different types of interconnects were investigated. Furthermore, stressed and unstressed samples were studied applying advanced physical analysis techniques in order to obtain additional information about the microstructure of the interconnects as well as interfaces and grain boundaries. These data were correlated to the observed degradation phenomena. Correlations of the experimental results to recently established theoretical models were highlighted.

Three types of Cu-based interconnects were studied. Pure Cu interconnects were compared to Al-alloyed (CuAl) and CoWP-coated interconnects. The latter two represent potential approaches that address EM-related reliability concerns. It was found that in such interconnects the dominant diffusion path is no longer the Cu/capping layer interface for interconnects as in pure Cu interconnects. Instead, void nucleation occurs at the bottom Cu/barrier interface with significant effects from grain boundaries. Moreover, the *in-situ* investigations revealed that the initial void nucleation does not occur at the cathode end of the lines but several micrometers away from it. The mean times-to-failure of CuAl and CoWP-coated interconnects were increased by at least one order of magnitude compared to Cu interconnects. The improvements were attributed to the presence of foreign metal atoms at the Cu/capping layer interface. Post-mortem EBSD investigations were used to reveal the microstructure of the tested samples. The data were correlated to the *in-situ* observations.

Kurzfassung

In dieser Arbeit wird eine Methode zur direkten Beobachtung der Elektromigration (EM) in Cu-basierten Leitbahnen vorgestellt. Das experimentelle Verfahren basiert auf *in-situ*-Untersuchungen im Rasterelektronenmikroskop. Die Bildung und Weiterentwicklung von Hohlräumen in mehrlagigen Teststrukturen aufgrund von Elektromigration kann in Echtzeit verfolgt werden. Unterschiedliche Leitbahntypen wurden auf diese Weise untersucht. Desweiteren wurden physikalische Analytikmethoden angewendet, um zusätzliche Informationen über das Gefüge und die Grenzflächen der Leitbahnen zu erhalten. Diese Informationen wurden mit den Beobachtungen aus den *in-situ*-Untersuchungen in Zusammenhang gebracht. Übereinstimmungen der experimentellen Ergebnisse mit aktuellen theoretischen Modellen wurden hervorgehoben.

Drei Typen kupferbasierter Leitbahnen wurden untersucht. Herkömmliche Kupferleitbahnen wurden mit Aluminium-legierten (CuAl) und CoWP-beschichteten Leitbahnen verglichen. Die letzteren beiden Typen stellen potentielle Alternativen dar, die Zuverlässigkeit zukünftiger Leitbahnsysteme zu verbessern. Es zeigte sich, daß in solchen Leitbahnen nicht die obere Grenzfläche zur Passivierungsschicht den dominierenden Diffusionspfad bildet, wie das in herkömmlichen Leitbahnen der Fall ist. Statt dessen wurde die Hohlraumbildung an den Grenzflächen zur Diffusionbarriere beobachtet. Der Einfluß von Korngrenzen wurde nachgewiesen. Desweiteren zeigten die *in-situ*-Untersuchungen, daß sich die ersten Hohlräume nicht am Kathodenende der Leitbahnen bildeten, sondern einige Mikrometer davon entfernt. Die mittlere Lebensdauer von CuAl- und CoWP-beschichteten Leitbahnen war mindestens eine Größenordnung höher als die von Kupferleitbahnen. Die Verbesserungen wurden dem Vorhandensein von Fremdmetallatomen an der oberen Grenzfläche zur Passivierungsschicht zugeschrieben. Anhand von EBSD-Untersuchungen wurde das Gefüge der getesteten Leitbahnen analysiert. Die Ergebnisse wurden mit den *in-situ*-Untersuchungen in Zusammenhang gebracht.

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Acronyms and symbols

ALD	Atomic Layer Deposition
BSE	Backscattered Electron
CMP	Chemical-Mechanical Polishing
CVD	Chemical Vapor Deposition
CoWP	Cobalt tungsten phosphide
CuAl	Aluminum-alloyed copper
EBSD	Electron Backscatter Diffraction
ECD	Electrochemical Deposition
EDS	Energy-dispersive (X-ray) Spectroscopy
EM	Electromigration
FIB	Focused Ion Beam
FSG	Fluorinated Silicate Glass
GPIB	General Purpose Interface Bus
HR-TEM	High-Resolution TEM
ILD	Interlayer Dielectric
IPF	Inverse Pole Figure
ITRS	International Technology Roadmap for Semiconductors
MTTF	Median Time-to-Failure
ND	Normal Direction
OBIRCH	Optical Beam Induced Resistance Change
PVD	Physical Vapor Deposition
RIE	Reactive Ion Etching
SE	Secondary Electron
SEM	Scanning Electron Microscopy
TEM	Transmission Electron Microscopy
TTF	Time-to-Failure

TXM	X-ray Transmission Microscopy
VFTL	Via-First-Trench-Last

A	Constant or cross-sectional area
D_0	Diffusion coefficient
D_B	Bulk diffusivity
$D_{barrier}$	Barrier interface diffusivity
$d_{barrier}$	Thickness of barrier interface diffusion path
D_{cap}	Capping layer interface diffusivity
d_{cap}	Thickness of capping layer interface diffusion path
D_{eff}	Effective diffusivity of metal ions
D_{GB}	Grain boundary diffusivity
d_{GB}	Thickness of grain boundary diffusion path
ΔR_{Joule}	Resistance difference due to Joule heating
$\Delta\sigma/\Delta x$	Stress gradient along interconnect line
ΔT_{Joule}	Termperature difference due to Joule heating
E	Electric field
E_a	Activation energy
F_e	Electrostatic force
F_{net}	Net force on a metal ion
F_p	"Electron wind" force
h	Line height
I	Electric current
j	Current density
J_{EM}	Atomic flux due to EM
k_B	Boltzmann's constant
k	Dielectric constant
L	Line length
l_c	Critical length
μ	Mobility of a metal ion
N	Atomic density
n	Current density exponent
Ω	Atomic volume
q	Electric charge

R	Electrical resistance
R_0	Resistance at reference temperature T_0
$R_{0.3}$	Resistance at 0.3 mA measurement current
ρ	Electrical resistivity
ρ_{defect}	Resistivity due to interaction of electrons with defects
ρ_{phonon}	Resistivity due to interaction of electrons with vibrating lattice
Rs	Sheet resistance
S	Slope of linear fit curve
T	Absolute temperature
T_0	Reference temperature (0 °C)
T_{EM}	Overall EM test temperature
t_{image}	Imaging interval
T_{melt}	Melting temperature
TCR	Temperature coefficient of resistivity
v_d	Drift velocity of metal ions
w	Line width
Z^*_{eff}	Effective charge number
Z_e	Charge number of a metal ion
Z_p	Charge number corresponding to electron wind

Chapter 1

Introduction

According to the 2006 International Technology Roadmap for Semiconductors (ITRS), the achievement of the required reliability of on-chip interconnects is one of the key issues for current and future technology nodes [1]. The continued reduction of interconnect dimensions and the introduction of new materials and processes create new challenges for the long-term reliability of semiconductor chips. Electromigration (EM) is one of the major reliability issues in Cu interconnects. The increasing current densities in complex designs, such as high-performance microprocessors (MPUs) lead to a continuous increase of the fundamental driving force for EM. Failures due to EM develop typically in the form of voids at the cathode end of interconnect segments and lead to resistance increases that compromises device functionality. Therefore, additional efforts are necessary to maintain EM reliability at the required level for future technology nodes.

In order to focus research and development efforts on the relevant aspects of interconnect fabrication, it is imperative to know the mechanisms for EM-induced degradation of interconnect structures. The impact of particular process steps and materials on the failure mechanisms needs to be explored. Investigating, understanding as well as modeling and ultimately controlling the failure mechanisms are important prerequisites to guarantee the reliability of semiconductor chips. Standard EM tests focus on the statistical evaluation of time-to-failure distributions from accelerated experiments of sets of samples. This approach is in particular useful for the determination of activation energies for the dominating diffusion mechanisms and for the extrapolation to lifetimes under operation conditions. Physical failure analysis methods are used to prepare and image cross-sections of the interconnect segments, after they failed. These data are important quality measures for the qualification

of manufacturing processes and for customer documentation. However, the early stages of EM-induced degradation of interconnects have to be studied during research and development of interconnect systems for new technology nodes. Knowledge about the initial void nucleation mechanisms is needed in order to tune processing in such a way that the void nucleation is delayed or even prevented.

This thesis provides a methodology for the investigation of EM in interconnects. An experimental framework based on *in-situ* scanning electron microscopy (SEM) investigations was developed for that purpose. It is capable to visualize EM-induced void formation and evolution in multi-level test structures in real time.

Three types of Cu-based interconnects were studied. Cu interconnects were compared to Al-alloyed Cu interconnects (CuAl) and CoWP-coated interconnects. The latter two represent potential approaches that address EM-related reliability concerns. Furthermore, stressed and unstressed samples were studied applying advanced physical analysis techniques in order to obtain additional information about the microstructure of the interconnects as well as interfaces and grain boundaries. These data were correlated to the observed degradation phenomena. Correlations of the experimental results to recently established theoretical models were highlighted.

Chapter 2

What is electromigration?

2.1 Fundamental mechanisms

EM in metals was extensively studied since the 1960s [2–13]. Especially the EM-related research in the semiconductor industry has generated a high degree of knowledge of this phenomenon.

Two forces affect metal ions in a conductor under the influence of an electric field. A direct electrostatic force F_e results from the electric field and has the same direction as the field. A second force F_p results from the transfer of momentum from the electrons onto the metal ions due to inelastic scattering. F_p is often referred to as the "electron wind" force. The combination of these two forces causes the motion of ions along the direction of the electron flow. The resulting mass transport is refered to as EM.

The net force F_{net} on a metal ion can be written as the sum of both forces:

$$F_{net} = F_e + F_p = (Z_e + Z_p) \cdot qE = Z^*_{eff} \cdot qE. \tag{2.1}$$

Z_e is the charge number of the metal ion, Z_p the charge number corresponding to the electron wind, q the electric charge, and E the electric field. Z_e and Z_p are usually combined to the parameter Z^*_{eff}, the apparent effective charge number, since the individual contributions cannot be measured separately. The mass flux resulting from the EM driving forces can be described by equation 2.2 [2]:

$$J_{EM} = N\mu F_{net} = N \cdot \frac{D_{eff}}{k_B T} \cdot Z^*_{eff} \cdot q\rho j \tag{2.2}$$

where J_{EM} is the atomic flux due to EM, N the atomic density and D_{eff} the effective diffusivity of the metal ions. k_B is Boltzmann's constant, T the absolute temperature, ρ the electrical resistivity and j the current density. The term

$$E = \rho j \tag{2.3}$$

corresponds to the electric field while the term

$$\mu = \frac{D_{eff}}{k_B T} \tag{2.4}$$

gives the mobility of the metal ions according to the Einstein relation. From the mass flux equation 2.2 the drift velocity of the ions, v_d, can be derived:

$$v_d = \mu F_{net} = \frac{D_{eff}}{k_B T} \cdot Z^*_{eff} \cdot q\rho j \tag{2.5}$$

The values for Z^*_{eff} and D_{eff} differ significantly, depending on the dominating diffusion mechanism for the conductor system (see also section 2.2).

In interconnect lines, the EM-induced mass transport leads to a concentration gradient that produces a stress gradient from one end of the line to the other. This mechanical stress effectively generates a backflow of metal ions in opposite direction to the current flow. This effect is commonly refered to as the Blech effect [8]. With the backflow stress taken into account, equation 2.5 is rewritten as follows:

$$v_d = \mu \cdot (F_{net} - \Omega \frac{\Delta\sigma}{\Delta x}) = \frac{D_{eff}}{k_B T} \cdot (Z^*_{eff} \cdot q\rho j - \Omega \frac{\Delta\sigma}{\Delta x}) \tag{2.6}$$

where Ω is the atomic volume and $\Delta\sigma/\Delta x$ is the stress gradient along the line. The stress gradient depends on the materials properties of the dielectric materials as well as the metal. However, with two counteracting contributions in this equation it can be deduced that the mass flux due to EM ceases under certain conditions. The net drift velocity will be zero under such conditions. This effect is often referred to as the "short length effect". A product of length and current density can be used to determine the critical length for a given current density:

$$(jl)_c = \Omega \cdot \frac{\Delta\sigma}{Z^*_{eff} q\rho} \tag{2.7}$$

with l_c being the critical line length of the particular test structure for a certain current density. The characterization of the critical product is very important as it can serve as a guideline to the designers of interconnect architectures. The utilization of line lengths less than l_c reduces the risk of EM failures significantly. In this study, however, the interconnects were much longer than the critical line length, so that the Blech effect can be neglected.

2.2 EM in Cu interconnects

2.2.1 Dual-inlaid process

In order to understand EM in Cu interconnects, the impact of the manufacturing process, materials and operating conditions have to be taken into account. Advanced Cu interconnects are manufactured using a so-called damascene or inlaid process [14]. The patterning starts with a continuous dielectric film that is patterned using optical lithography and a subsequent reactive ion etching (RIE) step. This approach requires lithographic masking in order to transfer the patterns onto the films. Trenches and holes are etched into the dielectric film, and subsequently, they are filled with Cu. The filled trenches serve as interconnect lines, while the filled holes form the vias that connect two interconnect levels vertically in stacked designs. There are two variations of the inlaid technology, single-inlaid and dual-inlaid process technology. While trenches and vias are fabricated in separate steps in the single-inlaid process, these steps are combined into one step in the dual-inlaid process. Figure 2.1 illustrates a typical via-first-trench-last (VFTL) dual-inlaid process flow, starting from a planarized Metal 1 surface.

Firstly, a continuous dielectric film stack is deposited. The stack consists of a thin etch stop layer (silicon nitride (SiN_x) or silicon carbide (SiC_x)), the actual dielectric film (fluorinated silicate glass (FSG) or low-k dielectric) and the via mask layer. The etch stop layer serves also as a diffusion barrier for the top interface of the underlying Metal 1. After optical lithography, RIE is used to etch the vias until the etch stop layer is reached. Next, the trench mask is transfered onto the wafer and the trenches are etched using RIE processes. During the final stages of the trench etch process, the etch stop layer at the bottom of the vias is removed as well.

Following the patterning, the metal deposition starts with the deposition of a diffusion barrier (typically Ta or TaN/Ta-bilayer) using a physical vapor deposition (PVD) process. This layer will prevent the Cu from diffusing out of the interconnect into the interlayer dielectrics (ILD) and towards the active regions of the devices. In a second PVD step, a thin Cu layer is deposited as a seed layer for the subsequent filling process. An electrochemical deposition (ECD, electroplating) process is used to fill the structures with Cu. Then, the wafer is completely covered by a continuous Cu film.

Next, a thermal annealing step is applied in order to recrystallize the Cu, thereby removing defects and forming larger grains. This step reduces the resistivity of the film and also drives impurities to the top of it. Subsequently, the excess Cu and barrier material is removed by chemical-mechanical polishing (CMP) of the wafer. The individual interconnect lines are thereby separated and the wafer is planarized. Depending on the chip design, the entire process flow is either repeated in order to form the next level of metallization or a thin capping layer (SiN_x or SiC_x) is deposited as final passivation of the chip.

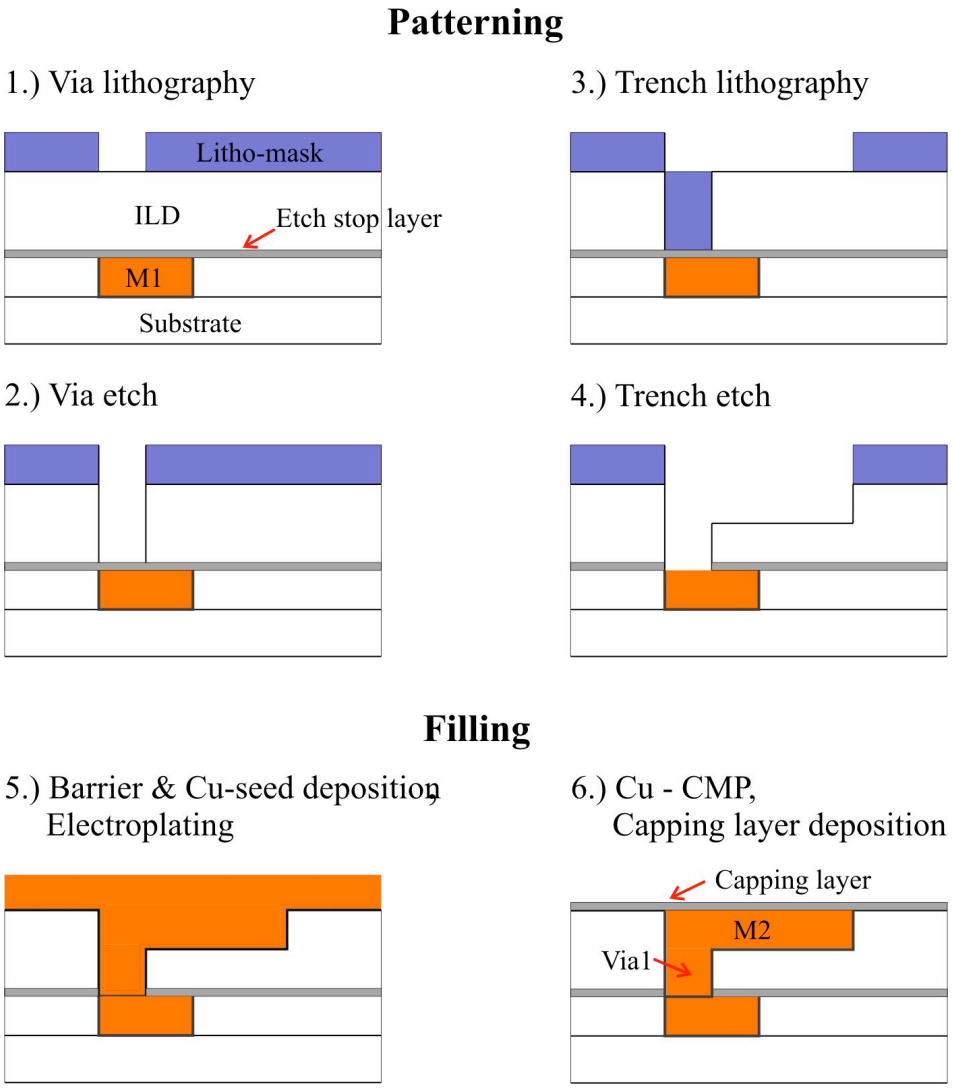


Fig. 2.1: Dual-inlaid process flow for Cu interconnect manufacturing.

2.2.2 Mass transport in Cu interconnects

Considering a mature processing technology, where no initial defects (i.e. voids or interface delaminations) are present, degradation of dual-inlaid Cu lines is related to a directed material transport [15]. A directed atomic transport requires the presence of a gradient of a physical parameter. A concentration gradient or more precisely a gradient on the chemical potential leads to interdiffusion, a gradient of the electrical potential, caused by a direct electric current, leads to EM. Temperature gradients cause thermomigration and stress gradients lead to stress-induced migration of atoms. Interdiffusion-related mass flow is described by Fick's first law [16]. Additional transport terms have to be added to the interdiffusion term for EM, thermomigration and stress-induced migration. In general, the formation of defects occurs due to local divergences in the mass flow. At such positions, the amount of incoming and removed material is not in balance. Local divergences in the mass flow are described by Fick's second law [16].

In pure Cu lines, there is no concentration gradient present. Therefore, interdiffusion does not need to be considered. The gradient of the electrical potential gives migrating atoms a bias towards the anode. It is proportional to resistance and current density. Temperature variations are possible during device operation, caused by locally increased current densities. That means, thermomigration is closely related to EM. Finally, stress gradients are mainly expected for via/line structures. Following these considerations, only EM- and stress-induced degradation phenomena will have to be considered. The effective diffusion coefficients and activation energies have to be discussed in relation to the geometry, the chemical composition as well as the microstructure and the interfaces of the interconnect.

For Cu interconnects, it is necessary to discuss the effective diffusion coefficient, D_{eff}, as the sum of several geometry-, interface- and microstructure-dependent contributions. Without initial defects, D_{eff} can be written as follows [17, 18]:

$$D_{eff} = D_B + \frac{d_{GB}}{L} D_{GB} + \left(\frac{2}{w} + \frac{1}{h} \right) d_{barrier} D_{barrier} + \frac{d_{cap}}{h} D_{cap} \qquad (2.8)$$

D_B describes the bulk diffusivity, D_{GB} the grain boundary diffusivity, $D_{barrier}$ the diffusivity along the Cu/barrier interfaces and D_{cap} describes the diffusivity along the top interface of a dual-inlaid Cu interconnect, also refered to as the Cu/capping layer interface. The factors d_i describe the "thickness" of the diffusion paths (i.e. grain boundary width or interface width). L is the

mean grain size, while w and h describe the width and height of the interconnect line, respectively. The microstructure along the line is non-uniform, meaning that the diffusion varies depending on the position along the interconnect line. Equation 2.8 assumes that an overall effective diffusivity can be described using an average parameter for the grain size (L). For low temperatures ($T < 0.5T_{melt}$) diffusion through the bulk of Cu crystallites can be neglected [19, 20]. Under these conditions, mainly diffusion along the grain boundaries and the interfaces contribute to D_{eff}.

The final assessment, which of the three remaining contributions, D_{GB}, $D_{barrier}$ or D_{cap}, forms the fastest diffusion path, depends significantly on the materials used in the on-chip interconnect stack, the used processes and process parameters. The fastest diffusion path will predominantly determine the lifetime of the interconnects. Only with a solid understanding of the main diffusion mechanism it is possible to modify the manufacturing processes in order to improve the EM reliabilty. Several process steps are known to have an impact on EM: The integrity of barrier and seed layers is crucial for the subsequent electroplating process. A good step coverage at the via corners as well as the via bottom is necessary for void-free Cu filling. However, the step coverage of the barrier and seed deposition processes depends significantly on the trench and via profiles. Sharp corners or a high line edge roughness have to be avoided during etching. Additionally, the post-etch and pre-barrier deposition clean processes have to remove etch residues at the sidewalls and the via bottom. CMP and capping layer deposition processes influence the quality of the top interface of metal lines to ensure strong adhesion between Cu and the capping layer. Generally, all process steps must be optimized to avoid initial defects such as voids or interface delaminations.

The fastest diffusion path can vary depending on the manufacturing technology and materials that are used to process the interconnects. For inlaid technology Cu interconnects, it was reported that EM is usually related to Cu transport along the interfaces (i.e. Cu/barrier interface diffusion in reference [21] or Cu/capping layer interface diffusion in references [20, 22, 23]. Looking at the majority of publications, it is commonly agreed that the degradation in inlaid Cu interconnects that are manufactured in the commonly used process of record with dielectric capping layers is dominated by diffusion along the top interface of the trenches, i.e. D_{cap} will have the largest impact on D_{eff}. Evidence was presented by Hu *et al.* [24], Hau-Riege *et al.* [22] and Meyer *et al.* [25], among others. Sometimes a bimodal distribution of failure times with a significant "early fail" behavior is reported for dual-inlaid interconnects, indicating a different mechanism.

In such cases, the "early failures" were attributed to process-related vulnerabilities of the vias in combination with a contribution of Cu/barrier diffusion [20, 26, 27].

Table 2.1 summarizes activation energies for potential diffusion paths in Cu interconnects. While these values are merely a selection of reported values, they underline the observation that the Cu/capping layer interface serves as the dominating diffusion path in Cu interconnects. There will be no significant impact of the microstructure as long as $E_a(\mathrm{Cu/SiN}_x) \ll E_a(\mathrm{Cu/grain\ boundary})$. However, if $E_a(\mathrm{Cu/SiN}_x) \cong E_a(\mathrm{Cu/grain\ boundary})$ can be achieved by strengthening the interfaces, then the microstructure of the interconnects will become important.

Table 2.1: Activation energies for potential diffusion paths in narrow Cu interconnects.

Diffusion path	E_a **[eV]**	**Reference**
Cu bulk	2.0–2.2	[28, 29]
Cu grain boundary	0.8–0.85	[30]
Cu/Ta barrier	1.4	[31]
$\mathrm{Cu/SiN}_x$	0.8	[32]

2.2.3 Microstructure effects

The influence of the microstructure on EM was studied extensively. While the implications for Al interconnects seem to be well understood, this is not entirely true for Cu interconnects. In Al interconnects, where the material transport occurs through grain boundary diffusion, it was shown that larger grains and a stronger <111>-texture of the films lead to improved lifetimes and tighter distributions [5]. For inlaid Cu interconnects, the relationship between microstructure and reliability is still a topic for experimental studies and model-based numerical simulations. Ryu reported similar results for inlaid Cu interconnects. In both cases, for Al and Cu interconnects, the improvement was attributed to a reduction of the number of flux divergence sites as well as the elimination of fast diffusion paths. Ryu compared chemical vapor deposited (CVD) Cu interconnects with electroplated Cu interconnects. CVD-Cu lines showed very small grains due to the conformal deposition in narrow trenches. Electroplated Cu lines, on the other hand, exhibited significantly larger grains after thermal treatment. As a result, CVD-Cu lines exhib-

ited shorter lifetimes and an early degradation for linewidths below 500 nm. Electroplated Cu lines showed longer lifetimes and no degradation for narrow linewidths [33, 34]. Hau-Riege *et al.* on the other hand reported that the influence of the grain size of inlaid Cu interconnects has almost no effect on the lifetime distribution [22]. This observation was attributed to the fact that diffusion along the top interface dominates the material transport in inlaid Cu interconnects and grain boundary diffusion does not play a major role.

There exist somewhat contradictory reports for the texture dependence of EM in Cu interconnects [34–36]. Nevertheless, the microstructure may affect the local diffusivity along the top interface to some extent. Several publications have shown that the diffusivity of Cu atoms across a Cu surface depends strongly on its crystallographic orientation [37–39]. Table 2.2 summarizes activation energy data for self-diffusion of Cu atoms across free Cu surfaces. The values vary significantly for different lattice planes and crystal orientations. It is worth to note that the activation energy for diffusion across free Cu(111) surfaces is significantly lower than that for the other orientations. The degree of Cu<111>-texture is often discussed in publications that are targeted on the influence of the interconnect microstructure on EM. However, in real interconnects, free Cu surfaces do not exist until voids are formed. Instead, the Cu surface is typically covered with a dielectric capping layer. Hence, the actual activation energies for interface diffusion will be different depending on the atomic structure and the chemical bonding of the interface and consequently the adhesion between Cu and the capping layer.

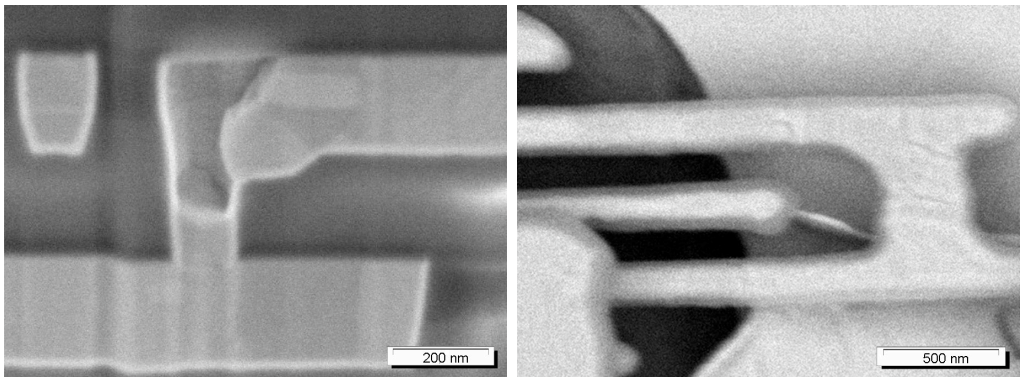
According to Lloyd *et al.* [40], the adhesion between capping layer and Cu depends on the orientation of the individual grains. The anisotropy of the elastic constants in Cu allows for considerable variation in the normal stresses at the interface. Consequently, the critical stress for delamination and hence for void nucleation depends on the orientation of the grains and on the stress gradients at grain boundaries. Once a void has been formed, a grain boundary between two grains with considerably different surface diffusivities will form a flux divergence site even though it does not act as a diffusion path itself. Additionally, although narrow Cu lines are considered to have a bamboo-like microstructure, there is a considerable amount of clusters of small grains present in such lines [41]. Such sites will also act as flux divergence sites, thereby locally controlling the propagation of voids along the top interface. Direct evidence of such phenomena was discovered by Meyer *et al.* and will be explained in detail in this thesis [25, 42].

Table 2.2: Activation energies for self-diffusion of Cu atoms across free Cu surfaces.

Lattice/direction	E_a **[eV]**	**Reference**
Cu(111)/n.a.	0.04	[37]
Cu(100)/n.a.	0.28–0.40	[38]
Cu(110)/$(1\bar{1}0)$	0.35	[39]
Cu(110)/(001)	0.84	[39]

2.2.4 EM-induced failures

Generally, two types of failures can occur in interconnects due to EM. Firstly, formation and growth of voids will lead to a locally increased resistance that degrades the functionality of the chip or cause open circuit failures. Secondly, the directed material transport may lead to the formation of hillocks or extrusions somewhere along the interconnect segment. Hillocks can form unintended electrical connections to neighboring lines, creating short circuits. In Cu interconnects, the via bottom plays a key role with respect to the formation of failures. With the diffusion barrier spanning across the bottom of the vias, the diffusion of Cu ions along the current path is effectively blocked. Therefore, via bottoms act as flux divergence sites. As a consequence, voids will form at cathode vias due to Cu depletion, creating a prefered site for open circuit failures. At anode vias, hillocks or extrusions could grow. Figure 2.2 shows a typical example of void and extrusion formation in Cu-interconnects.



(a) Void at cathode via (cross-section). (b) Extrusion at anode via (top-view) .

Fig. 2.2: Void and extrusion formation in Cu interconnects.

Hu *et al.* have proposed a method to reduce the effect of the via bottom by deliberately employing a very thin barrier at the via bottoms. Such test structures exhibited extremely long lifetimes. The effect was explained with the migration of Cu atoms through the thin via bottom barrier [24]. This approach has two distinct disadvantages that prevent the implementation in real product designs. Firstly, the short length effect can not be used as a design rule, where interconnect segments are deliberately drawn shorter than the critical length according to equation 2.7 in order to completely eliminate EM. Secondly, the expected failure sites at cathode vias may shift to unpredictable positions along the current path of a given design. Both issues would complicate interconnect design and reliability modeling.

The formation of hillocks is initially prevented in Cu interconnects due to the rigid confinement by the surrounding dielectrics. However, at a certain level the EM-induced mechanical stress may cause delamination and cracking of the capping layer interface. Then the formation of hillocks becomes possible. Especially Cu interconnects embedded in low-k dielectrics may exhibit such a behavior since the mechanical stiffness is reduced compared to interconnects embedded in FSG [43].

2.3 Approaches for improving EM reliability

The research efforts to improve the EM resistance of Cu interconnects have focused on at least three approaches: alloying of Cu similar to Al interconnects, plasma-chemical treatments of the Cu surface prior to dielectric deposition and deposition of additional metallic capping layers.

2.3.1 Alloying of Cu interconnects

The influence of the addition of the alloying element on microstructure, resistivity, EM-based reliability as well as the manufacturability of Cu interconnects was studied in a number of publications [44–49]. In several studies a wide variety of potential alloying elements such as Ag, Al, In, Mg, Mn, Sn, Ti, and Zr were explored. Several ways were suggested on how to introduce the alloying element into the Cu. Mainly, modified PVD processes were developed to deposit the alloying element together with the Cu seed layer that is necessary for the Cu electroplating process to fill the trenches. Separate targets can be used, resulting in a stacked seed layer with the alloying element forming an additional layer. Alternatively, alloyed sputter targets can be used

in order to obtain a Cu-alloy seed layer. During Cu plating and subsequent thermal treatments, the alloying element diffuses out of the seed layer into the bulk of the Cu lines. All references state an increase in lifetime for certain concentrations of the alloying elements. It was found that the alloying elements are localized at the grain boundaries or at the top surface of the lines after annealing. In some alloys precipitates are formed. Activation energies were in the range of 1.4 eV [45, 49]. This is comparable to the value for Cu/barrier diffusion. While these findings are promising in terms of EM performance, most papers also state that the resistivities of the films were increased to some extend. In some cases the resistivity of the as-deposited films could only be reduced by very long thermal treatments (hours) at very high temperatures. These are major limitations in terms of product performance and manufacturability .

A recent approach was presented by Koike *et al.* [50]. In this case, self-forming barrier layers using CuMn alloy thin films were investigated. The CuMn alloy films were deposited directly on the structured dielectric substrate. After annealing, a very thin amorphous manganese oxide layer was formed uniformly at the interfaces. Mn had been diffused out of the metal film completely, leading to a very low resistivity. Furthermore, the thin oxide layer exhibited good diffusion barrier properties against Cu diffusion. The EM performance was also improved compared to conventional Cu interconnects. However, this may be because of similar effects as discussed in reference [24], as the images presented by Koike indicate that the Cu grains seem to extent from Metal 1 up into Via 1. That means, there is no effective diffusion barrier present at the via bottom. While it would provide a very attractive way to improve both, EM reliability and via resistance by removing the barrier layer at the via bottom, it creates new challenges for circuit designers and integration engineers. Removing the flux divergence site at the via bottom might push the failure sites to other less controllable regions of the circuit. Furthermore, the short length effect cannot be implemented as a design rule in order to eliminate EM completely.

2.3.2 Cu surface treatments

Another approach for strengthening the top interface of inlaid Cu interconnects is the plasma-chemical treatment of the Cu surface prior to the deposition of the dielectric capping layer. Vairagar *et al.* have studied the effect of various plasma-chemical treatments such as NH_3 treatment, H_2 treatment and silane treatment [51]. The different treatments resulted in improved EM life-

times. This effect was generally attributed to an improved adhesion between the dielectric capping layer and the Cu. In the case of the NH_3 treatment, this strengthening of the interface is explained with the reduction of Cu oxide and the formation of CuN_x. Hydrogen plasma treatments effectively clean the surface, which also leads to improved adhesion. The improvements after a silane treatment of the samples were attributed to the formation of silicides on the Cu surface. Cu/silicides would pin the Cu atom at their position, thereby reducing their mobility.

2.3.3 Metallic surface coatings

The most significant improvement of the EM reliability so far was achieved by the selective deposition of metallic capping layers on the Cu surface of interconnect lines. As explained by Lane *et al.* [32], the nature of the interfacial bonding seems to be critical for adhesion and EM resistance. Metallic capping layers should result in significantly enhanced EM reliability, compared to other types of surface modification.

Hu *et al.* have studied the effect of several metallic coatings, such as CoWP or Ta/TaN [23, 31]. Especially the samples with a CoWP-coating showed no abrupt resistance increase even after test times of more than one thousand hours. In comparison, the samples with a Ta/TaN capping layer showed an abrupt line resistance increase after several hundreds of hours, while the reference samples with a dielectric capping layer failed after less than 20 hours. The samples were stressed at temperatures between 250–377 °C and a current density of $3.5\,\mathrm{MA/cm^2}$. Yan *et al.* reported similar results for samples that were coated with CuSn, using an immersion process [52]. The reported activation energy of 2.0 eV for narrow CoWP-coated interconnects with a bamboo-like Cu microstructure is in the range of that for Cu bulk diffusion. These data indicate that interface diffusion was significantly reduced and is not the dominating material transport process anymore. For wide lines with a considerable amount of grain boundaries aligned with the current direction, the activation energy was close to 1 eV. That means, the major material transport occurs through grain boundary diffusion [29].

The most promising technology approach has become selective electroless CoWP deposition. However, there is a number of challenges connected to this technology. It was found, that the growth rate depends on the orientation of the Cu grains. More critically, contamination of the dielectric surfaces between adjacent lines with metal is an issue that has to be avoided [26, 53]. Otherwise, increased interline leakage would degrade the product performance

considerably. A slight increase of the resistance of CoWP-coated Cu lines during EM testing has also been reported [23]. The extent of this increase is relatively small. It would not lead to severe failures, but it could provide a risk for the long-term functionality of products, especially for speed-critical designs such as high-performance microprocessors. However, it seems that this effect can be avoided by smart processing [26].

2.4 Characterization techniques for EM in interconnect structures

Under typical operating conditions of microprocessors, EM-related failures develop only after very long times, i.e. several years. However, it is imperative to assess the EM-based reliability of interconnect structures before they are implemented into real products. Otherwise, long-term reliability can not be guaranteed. A number of different techniques were suggested. Vairagar provided a summary in [54]. Two of these methods are more widely used, the accelerated lifetime test method and the drift velocity method.

2.4.1 Accelerated lifetime test method

For this test, sets of samples are stressed under accelerated conditions. The temperature and the current density are chosen well above the potential operating conditions. The test temperatures range typically from 250 °C to 350 °C, and the current density is chosen in the MA/cm^2 range. Under such conditions the test time can be reduced significantly. For typical Cu interconnect test structures it will range from several tens to hundreds of hours. During the test, the resistance of the samples is continuously monitored and the time to failure is recorded. Failure criterions can be either a certain increase in resistance (typically 10 to 20 %) or the development of shorts with adjacent monitoring structures. A lognormal distribution is commonly employed for time-to-failure statistics in reliability engineering [55, 56]. Two statistical parameters can be extracted in order to compare different sets of samples with each other: the median time-to-failure (MTTF, time for 50 % of the samples failed) and the standard deviation of the lognormal distribution (σ, the width of the distribution). More details about the application on failure statistics of Cu interconnects can be found in the PhD theses of Hauschildt and Vairagar [54, 57].

Black found an empirical equation, that relates MTTF to the experimental conditions as well as providing a link to the dominating diffusion mechanism [4]:

$$MTTF = Aj^{-n} \cdot e^{(E_a/k_BT)} \tag{2.9}$$

where A is a constant which contains a factor involving the cross-sectional area of the interconnect, j the current density and n an exponent that describes the dependency of the failure mechanism on the current density. n ranges from 1 to 2, with typical values being closer to 1. E_a is the activation energy of the dominating diffusion mechanism. E_a and n can be determined by testing several sets of samples at different temperatures and current densities, respectively. n was found to be close to 1 for Cu interconnects [58,59]. Black's equation can then be used to predict the lifetime under operating conditions by extrapolating from the test conditions, assuming the same solid-state physical mechanisms cause degradation and failure.

The accelerated lifetime test method is nowadays widely used as standard method to characterize EM, and in industry for development and qualification of manufacturing technologies. It can be performed on wafer-level inside the production environment or as an oven experiment using packaged test samples. In the latter case, heating is achieved by applying high current densities in the MA/cm^2 range.

2.4.2 Drift velocity method

The drift velocity method employs a test structure designed by Blech [7] to measure the EM-induced mass transport directly. Blech used a strip of metal deposited over another strip of highly resistive metal as test structure. This design ensures that the current mainly passes through the strip to be tested. Such test structures are also known as Blech structures. During current stressing, the material is transported along the strip, leading to depletion of the metal at the cathode end and accumulation near the anode end. An average drift velocity is obtained by measuring the depletion at the cathode end and the time of stressing. From this data, the critical product $(jl)_c$ of current density and length can be determined. Utilizing equation 2.6 and with

$$D_{eff} = D_0 e^{-(E_a/k_BT)} \tag{2.10}$$

being the temperature-dependent effective diffusion coefficient, it is possible to determine the activation energy E_a, if the test is performed at several temperatures. Measuring the drift velocity as a function of the stress current

density, it is also possible to determine the product $D_{eff}Z^*_{eff}$, according to equation 2.5. Although the original Blech structure is very different from dual-inlaid Cu interconnect structures, it is possible to apply this method to Cu interconnects. Thrasher *et al.* have studied the Blech effect in single-inlaid Cu lines [60].

2.4.3 Dynamic observation – *in-situ* techniques

In addition to the methods described above, it is also possible to use *in-situ* techniques to observe EM-induced degradation phenomena in interconnects directly. Such techniques are particularly useful in exploring the early stages of the degradation, where no electrical signals such as significant resistance changes, are measurable. Initial void formation sites as well as the impact of the metal microstructure on the material transport and the virtual void movement can be observed directly. *In-situ* investigations give valuable insight into the fundamental failure mechanisms, thereby helping to understand particular EM behavior such as early failures. SEMs are most commonly used for *in-situ* studies [25, 44, 61–65], but also *in-situ* transmission electron microscopy (TEM) studies [35] and *in-situ* transmission X-ray microscopy (TXM) studies [66] were reported. The careful choice of the test structures and the preparation of the samples are the key challenges for successful investigations.

SEM-based techniques are especially useful to study surface or interface related phenomena. Moreover, these techniques are less restrictive on the physical sample size, making it possible to study fully-passivated interconnects. TEM-based techniques are especially useful to study atomic transport mechanisms across lattice planes with near-atomic resolution. However, the investigation of fully-embedded real interconnects is difficult due to the limited space for samples within the microscope. With the TXM-based technique it is possible to study the void evolution within the bulk of fully embedded interconnects lines in addition to the interfaces. The spatial resolution of this method depends on the radiation source. A resolution of about 20 nm is possible with a synchrotron radiation source, while laboratory-systems are capable of achieving about 60 nm spatial resolution.

2.4.4 Numerical simulation of EM in interconnects

A complementary approach to the experimental investigation of EM in interconnects is the numerical simulation of void nucleation and evolution based on theoretical models. Physics-based modeling can help to understand the fundamental mechanisms involved in EM. The interaction of several contributing factors to reliability-limiting degradation processes such as geometry, materials and process parameters as well as their importance could be explored. Simulations are useful to plan experiments more effectively in order to reduce experimental efforts and learning cycles.

Sukharev *et al.* proposed a complex model and simulation algorithm to predict EM-induced stress evolution in interconnects as well as for the three-dimensional simulation of void nucleation and evolution [67–69]. The model incorporate all important atomic driving forces, such as stress gradients, thermal gradient, vacancy concentrations as well as different diffusivities along interfaces and grain boundaries. The model allows the simulation of EM-induced degradation in multi-level interconnect segments with different dominating diffusion paths, depending on the interconnect microstructure. Some of the experimental results from this thesis were used to verify the simulation results.

Chapter 3

Experimental procedures

In this study, *in-situ* SEM investigations were performed on several types of on-chip interconnects in order to obtain a time-resolved visualization of the EM-induced generation of voids and their subsequent propagation and growth. The *key point of the entire experimental procedure* is, that the studied interconnects remained completely embedded within the surrounding ILD materials and, at the same time, electron imaging was performed on cross-sections of such structures. In order to realize this, a complex sample preparation and experiment procedure had to be developed.

Additional analytical methods, such as TEM in combination with energy dispersive X-ray spectroscopy (EDS) and SEM in combination with electron backscatter diffraction (EBSD) at cross-sections, provided information about the sample conditions after an *in-situ* experiment was finished, i.e. the position of voids relative to the interfaces or the Cu microstructure.

For the alloyed Cu interconnects that were investigated the spatial distribution of the alloying element within the Cu line was of additional interest, since it has an impact on the resistivity of the conductor material. For each type of interconnects reference samples were taken and characterized without EM stressing.

3.1 Samples

Three types of interconnects were investigated in this study:

- pure Cu interconnects.
- Al-alloyed Cu interconnects (CuAl).
- Cu interconnects with
  cobalt tungsten phosphide surface coating (Cu/CoWP)

3.1.1 General characteristics

The Cu samples and the CuAl samples were fabricated in 130 nm dual-inlaid technology using FSG as dielectric material and SiN_x as trench etch stop and capping layers. The CoWP-coated samples were fabricated in 130 nm single-inlaid technology. Ta-based barriers were used in all samples. The samples were taken from scribelines of full-flow production wafers, that contained 8 layers of metallization, except for the CoWP-coated interconnects. These sample were taken from short-flow wafers with only 4 layers of metallization. The wafer scribelines contain a variety of test structures that are used for production monitoring purposes. EM test structures and resistance monitoring test structures, which were used for this study are included. Table 3.1 summarizes the general characteristics of the interconnects as well as the manufacturing processes used.

All wafers have received the thermal budget of the entire production process up to the point where the wafers were ready for assembly. The interconnects in the samples can be assumed to be identical to the interconnects in the microprocessor product itself.

3.1.2 Fabrication of CuAl interconnects

In order to improve the EM lifetime, Cu interconnects samples were alloyed with Al. In this study, the alloying element was introduced during the Ta-barrier deposition process. This approach is different to other studies where the Cu seed deposition process was modified. In order to provide an easy way of evaluating this new approach, a Ta sputter target was deliberately driven over the end of its lifetime, until the Al back plate was partly exposed. As a consequence, Al was deposited on the wafer together with Ta yielding

Table 3.1: General characteristics of the interconnect types.

Interconnect type	**Cu**	**CuAl**	**Cu/CoWP**
Technology	130 nm dual-inlaid	130 nm dual-inlaid	130 nm single-inlaid
Trench/via ILD	FSG	FSG	FSG
Capping layer (ILD)	SiN_x	SiN_x	SiN_x
Trench etch-stop	SiN_x	SiN_x	SiN_x
Barrier + Seed	Ta + Cu PVD-deposited	TaAl + Cu PVD-deposited	Ta + Cu PVD-deposited
Metal	Cu ECD-deposited	Cu ECD-deposited	Cu ECD-deposited
Metallic coating	–	–	CoWP electroless

a mixed TaAl layer [70, 71]. The concentration of Al within this layer was in the range of 1 to 10 at.-%. Figure 3.1 provides a scheme of the metal deposition sequence for CuAl interconnect fabrication. Al is introduced by depositing a mixed TaAl barrier (1.), followed by Cu seed deposition (2.) and Cu electroplating (3.).

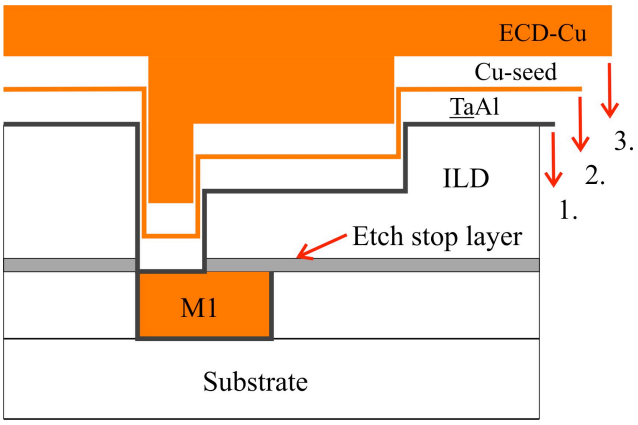


Fig. 3.1: Introduction of Al during CuAl interconnect fabrication.

The Cu seed and ECD-Cu deposition processes remain unchanged to standard processing. An advantage of this approach is that there exist a number of alternative barrier deposition techniques, such as PVD, CVD, atomic layer deposition (ALD) or self-forming barriers which may be adopted for the introduction of alloying elements during barrier deposition.

3.1.3 EM test structures

In order to perform *in-situ* SEM investigations of EM-induced degradation of interconnects it is essential to have some pre-information about the potential failure site, since the field-of-view of the SEM is limited. For instance, at a SEM magnification of 20.000x the field-of-view is only 5.85 μm wide, while the interconnects can be several hundreds of μm long. There is a certain type of test structure that is widely used for the investigation of EM in multilayer structures in oven experiments. The principle design of such test structures is shown in figure 3.2.

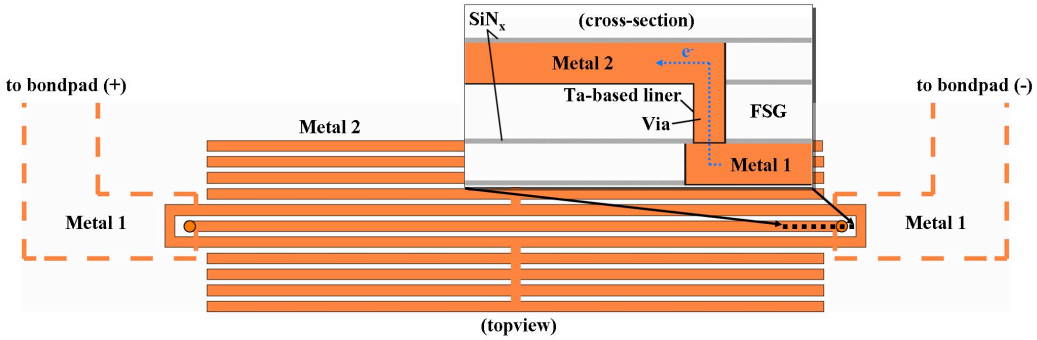


Fig. 3.2: Layout of EM test structure - Top-view and cross-section.

The structures usually consist of an array of metal lines with the center line being the line under test. The metal lines next to the center line usually form a ring and serve as extrusion monitors. Extrusion failures due to the formation of leakage paths or shorts between the two neighboring lines may thus be detected. Depending on which level of metalization is tested, the line array resides either in Metal 1 or Metal 2 for a two-level design. When Metal 1 is tested (downstream configuration), the connecting wide metal lines (dashed lines) are in Metal 2 and the line under test is connected by one via at each end of the line. When Metal 2 is tested (upstream configuration), the connections to the bond pads are in Metal 1. In the case of the dual-inlaid technology, the vias at the ends of the line are part of the structure under test. The fact that the vias at the end of the line belong to the structure under test for Metal 2 is quite important for the EM degradation mechanism and for destructive failure analysis after EM experiments.

The inset in figure 3.2 shows a schematic cross-section of the EM test structure. This area corresponds to the region of interest for the *in-situ* SEM observations, that was imaged during the experiments. For all experiments of this study the samples were tested in upstream configuration. The electron

current flow is then upwards and to the left as indicated by the blue arrow in figure 3.2. Table 3.2 summarizes the physical dimensions of the test structures. Metal 5 was tested for Cu as well as CuAl samples and Metal 2 for Cu/CoWP samples.

Table 3.2: Physical dimensions of the EM test structures.

Interconnect type	**Cu**	**CuAl**	**Cu/CoWP**
Tested metal layer	M5	M5	M2
Width x Height [μm]	0.38 x 0.38	0.43 x 0.40	0.20 x 0.51
Via diameter [μm]	0.35	0.35	0.20
Line length [μm]	800	800	800

3.2 Setup for *in-situ* SEM investigations

In contrast to other *in-situ* studies [44, 61, 63, 65], the experimental setup for the *in-situ* SEM investigations used in this study was designed to fulfill a number of prerequisites:

- The interconnects should remain fully passivated without any damage to the interfaces.
- Cross-sections should be imaged since the analysis of multi-level interconnect structures is of special interest.
- The setup should be capable of sample heating up to 400 °C with reasonable temperature stability.
- The experiments should run highly automated, including drift correction, image recording as well as resistance monitoring.
- The setup should be optimized for best-possible imaging conditions.
- Subsequent failure analysis with advanced analytical techniques (i.e. SEM/EBSD or TEM/EDS) should be possible.
- Identical samples as used for accelerated lifetime test in oven experiments should be used in order to ensure comparability of the results.

The setup was first described by Meyer *et al.* [25].

3.2.1 Sample preparation and assembly

Cross-section preparation

The key to success of the *in-situ* experiments lies apart from other factors in the careful preparation of the samples. Two aspects were considered: best possible access to the area of interest for the electron beam and the guaranteed integrity of the interconnect. From the imaging point of view a flat cross-section directly through the interconnect and parallel to the lines is prefered. This approach, however, would destroy three of the four interfaces of the metal line and affect the electrical functionality. Instead, the cross-section is placed in front of the tested interconnect line. In order to have complete control about the exact position of the cross-section and the integrity of the interfaces, a three-step procedure was established. Figure 3.4 provides an illustration of this procedure.

Initially, a strip of silicon, approximately 3 cm x 1 cm in size, is cleaved out of the wafer. The desired test structure has to be placed in the center of this strip with the Cu lines running across the silicon piece parallel to its narrow side. Next, the sample is fine cleaved exactly parallel to the Cu lines and in a distance of not more than 30 μm away from the test structure. This step is done using an automated cutting or cleaving tool. In this case, a Disco dicing saw DAD321 was used. It utilizes a fast rotating diamond blade ($\approx$10.000 rpm) that can be aligned very accurately to the sample. The resulting cuts are less than 50 μm wide and margins of around 10 μm to the test structure are possible without damage. The surface topography of the cross-section after cutting is relatively smooth (less than 1 μm RMS roughness), and no delaminations were observed.

The mechanically cleaved sample has up to 30 μm of excess material in front of the metal line to be imaged. This material has to be removed with caution as to avoid damage to the interfaces of the interconnect line. The preparation of the final cross-section was done by means of focused ion beam (FIB) milling. A FEI Dualbeam FIB Strata 235 instrument was used for this task. Typically, a coarse FIB-cut of about 25 μm in width is prepared first, leaving at least 1 μm of remaining material in front of the line. An ion beam current of up to 20 nA is applied in a cross-section cleaning pattern instead of a coarse pattern that is usually used for such pre-cuts. This procedure ensures a flat surface of the FIB cross-section. A cross-section cleaning pattern moves the ion beam line-by-line successively towards the cross-section while a coarse pattern typically irradiates the entire area at once.

In order to enable additional post-mortem EBSD analysis, some geometrical requirements for the access to the area of interest have to be considered. The EBSD technique as well as the sample requirements related to the investigation of Cu interconnect, both from top-down and at the cross-section, were explained in detail in [41]. While the FIB-cuts provided good access of the primary electron beam, the escape path of the backscattered and diffracted electrons towards the EBSD detector screen was partly blocked by the sidewalls and the bottom of the FIB-cuts. In order to overcome this limitation, the samples were mounted upside down in the SEM chamber with the cross-section surface tilted 70 ° relative to the horizontal axis. In order to be able to use the samples for EBSD in this position, the FIB-cut has to be very deep. Otherwise the bottom of the FIB-cut would block the primary electron beam. For a distance of the FIB-cut of 30 μm away from the sample edge a depth of 80 μm is necessary to perform an EBSD analysis. Figure 3.3 illustrates the sample position inside the SEM chamber.

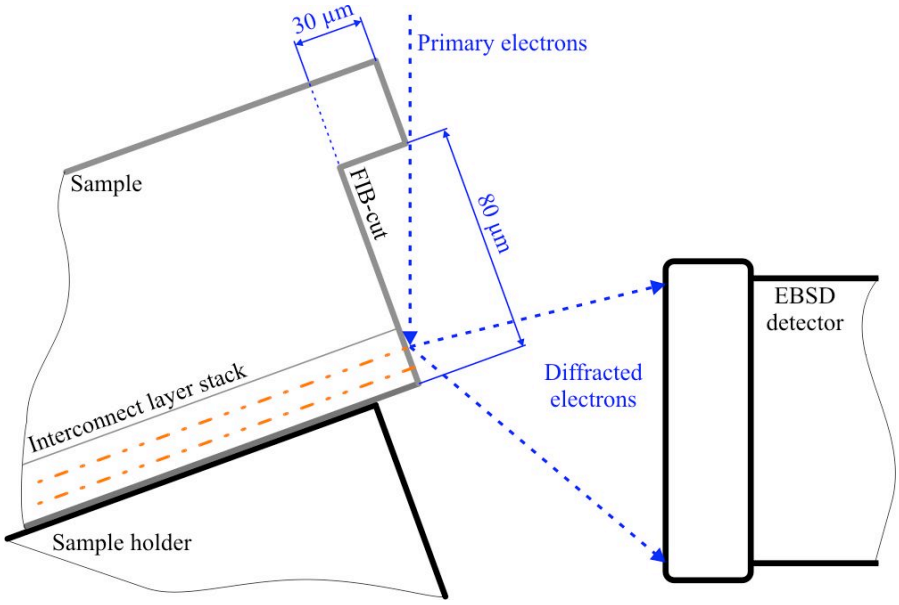
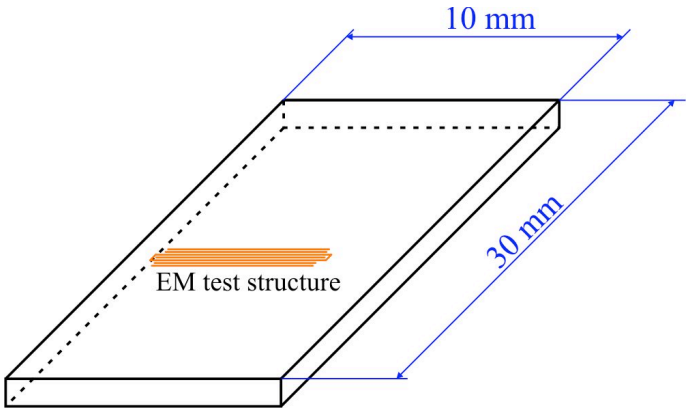


Fig. 3.3: Sample mounting for EBSD analysis of EM-stressed samples.

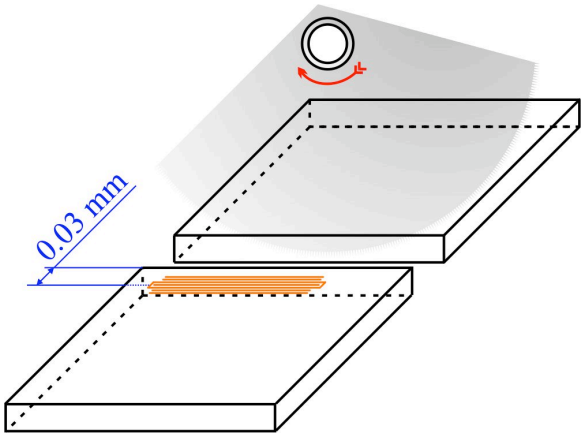
The most challenging part of the entire procedure is the preparation of the final cross-section. It is crucial to cut as close as possible to the metal line of interest in order to achieve a reasonable image quality during *in-situ* SEM imaging but leave enough ILD in front of it in order to guarantee the integrity of the interfaces. One constraint is the spacing between two adjacent interconnect lines. All lines of the array on one side of the tested line have to be removed including the extrusion monitor line in order to gain access with the electron

beam. For the used test structure this line-to-line spacing is about the same as the linewidth (table 3.2). However, the experiments have shown that it is necessary to have a much thinner passivation left on the cross-section in order to achieve the desired image resolution and to limit image artifacts due to negative sample charging to a minimum. A thickness of about 80 nm is desirable, while a thickness of 150 nm was found to be the upper limit.

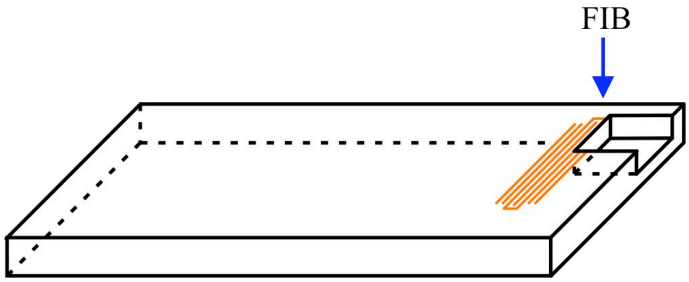
The final FIB-cut is prepared using a much lower ion current of 500 pA. Again, the ion beam is moved line-by-line towards the sample. The distance between two adjacent FIB lines is typically below 20 nm. A line exposure time of about 10 seconds is sufficient. The cross-section is continuously monitored with the SEM, and special attention has to be paid to the moment when to stop cutting. An electron acceleration voltage of 3 to 5 keV was chosen, and the detection system is set to backscattered electron imaging. The low electron energy limits the information depth to a minimum. The usage of backscattered electron imaging removes image artifacts due to sample charging and provides good materials contrast between light materials (ILD - dark) and heavy materials (metals - bright) [72]. With these beam settings the embedded metal line is not visible until the remaining passivation thickness is in the range of 100 nm. Once the first faint signs of it appear, the risk to damage the interconnect increases with each successive FIB line. Only two or three more FIB lines can be cut then. In figure 3.5, a secondary electron (SE) image and a backscattered electron (BSE) image of the final FIB cross-section are also given. The SE image represents the images that are taken during actual *in-situ* experiments. In the BSE image, the interconnect line of interest is just becoming visible. At this time, the final FIB-cut has to be stopped. The sample preparation is completed.



(a) Silicon strip with EM test structure.

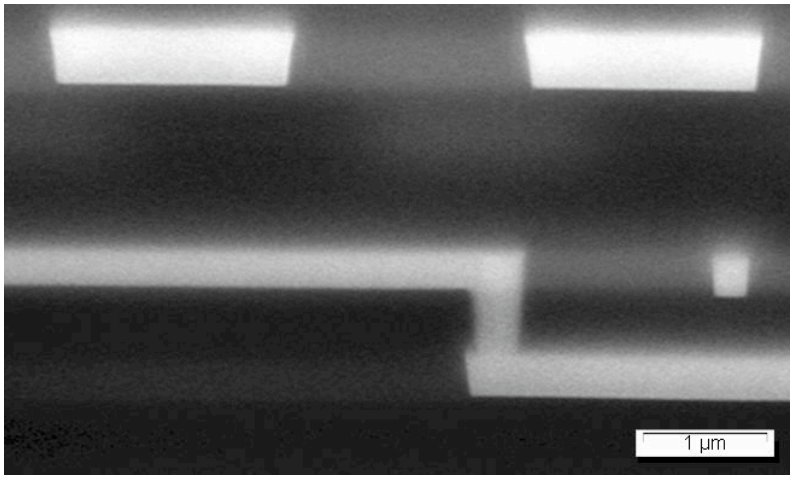


(b) Coarse cleaving parallel to EM test structure.

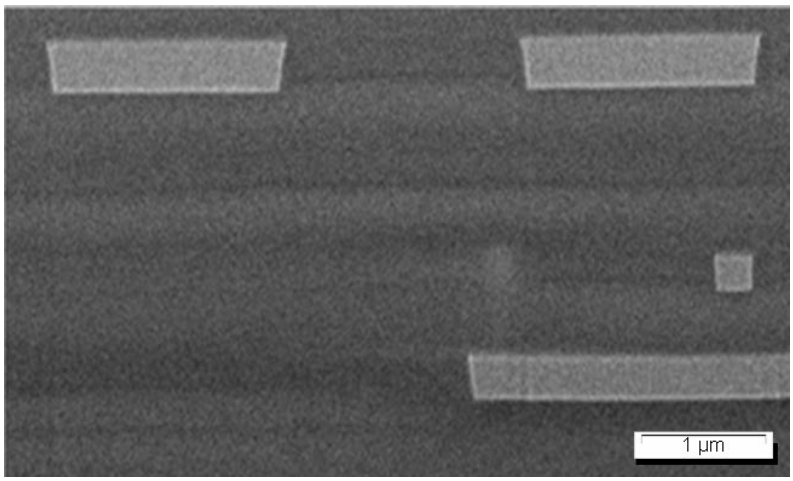


(c) FIB preparation of final cross-section.

Fig. 3.4: Sample preparation procedure.



(a) SE image of FIB cross-section at 20 keV.



(b) BSE image of FIB cross-section at 5 keV.

Fig. 3.5: SEM images of the final FIB cross-section at different primary beam energies and different electron detectors.

Assembly

In order to establish the electrical connections to the test structure, modified test chip packages were used. Such packages with 24 pins are commonly used in oven experiments. For the *in-situ* samples, the packages were cut lengthwise into two halves. A sample is then attached to the package using silver paint with the FIB-cut parallel to the open side. Two gold bond wires provide the electrical connection to selected pins of the package. The advantage of this kind of assembly is that open access to the FIB-cut for angles from 0 to 90 ° relative to the sample normal becomes possible.

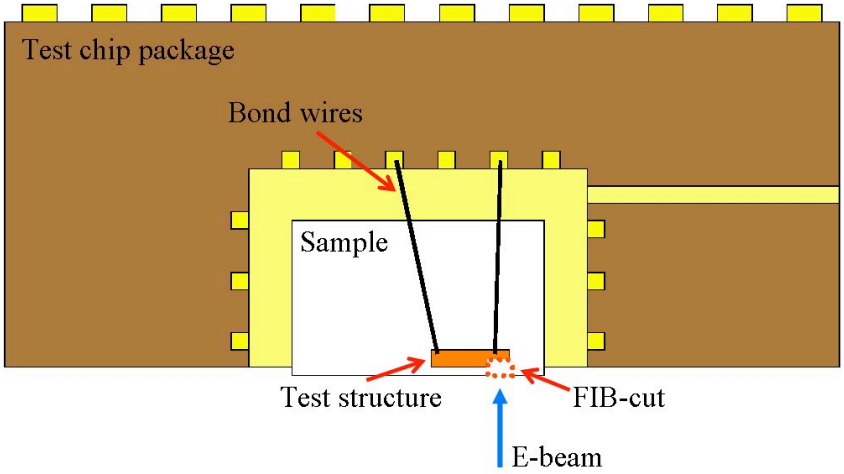


Fig. 3.6: Mounting of samples on modified 24-pin test chip package.

3.2.2 Experimental setup

Electron microscope

A LEO Gemini 1550 field-emission scanning electron microscope was used for the experiments. The electron column of this type of microscope does not form external electromagnetic lenses between the pole piece and the sample chamber. This is an important prerequisite for the modification of the sample holder in order to incorporate the sample heating system. The SEM is equipped with two electron detectors, an InLens-detector and an Everhardt-Thornley-type chamber detector (SE2) [72]. The InLens-detector resides inside the electron column and is designed to detect secondary electrons (so-called SE1 electrons) to enable higher spatial resolutions. It is usually the

detector used for high-resolution imaging. The chamber detector detects a broader energy range of secondary electrons (SE1 + SE2) as well as a considerable portion of backscattered electrons (BSE) [72]. Depending on the sample conditions, it is usually less susceptible to charging of the sample and can be adjusted in order to change the secondary to backscattered electrons ratio by modifying the collector grid voltage between -250 V and 400 V. There is no image shift associated with the switching between both detectors. This is important for the automated sample drift correction procedure.

Typical imaging conditions for this type of instrument are an acceleration voltage of 5 keV and a beam aperture of 30 μm using the InLens detector. However, for the *in-situ* investigations it was necessary to use a higher beam voltage and current in order to achieve a better penetration through the passivation and to reduce image noise due to sample charging. Table 3.3 summarizes the imaging conditions that were used for *in-situ* SEM experiments.

Table 3.3: SEM imaging conditions used during *in-situ* experiments.

Parameter	**Setting**
Beam voltage:	20 keV
Beam aperture:	30–120 μm
Beam current:	$\approx$ 0.3–5 nA
Detector (reference/search image:	SE2
Scan speed (reference/search image):	5
Detector (final image):	InLens
Scan speed (final image):	9

Reference and search images were captured at a faster scan speed to save time. They were used during the automated sample correction routine. The final images were captured at a much slower scan speed in order to reduce the image noise.

Sample heater

This section outlines the sample heating system that was designed for the LEO Gemini 1550 SEM. Main focus was put on simplicity, robustness and low costs. Another important aspect was the minimization of thermal expansion due to temperature fluctuations at the sample position. This thermal stability is necessary in order to keep the mechanical sample drift at a minimum.

It was accomplished by a symmetrical design and the careful choice of materials. Additionally, it was important that the precision and stability of the original 5-axis stage of the SEM was not compromised. High-resolution imaging and long-term analyses such as EBSD require extreme stability of the sample relative to the electron beam.

In order to avoid a damage of the precise mechanics of the tilt, rotation and Z axis of the stage, these components were completely removed. The remaining XY base provided a good basis for a custom-made sample stage. A special sample heater was designed and built to fit onto this base[1]. It consists of four components:

- The base plate is rigidly attached to the XY stage with three screws. It can be easily adopted to other stage types.
- The ceramic mounting post serves as support for the heat shield and the heating head. It fits into the central mount of the base plate. The material has a low thermal conductivity, which helps to reduce the heat load on the XY base.
- The purpose of the circular heat shield is to reduce the radiation heat load on the XY mechanism. Additionally, it serves as tray for cables and clamps.
- The main component of the sample heater is the heating head. It is mounted at the top of the ceramic post and can be adjusted manually in height in order to set the desired working distance between the sample and the pole piece of the SEM. Additionally, a manual tilt mechanism is built in. The heating head can be tilted $\pm$ 90 ° in order to set the desired sample viewing angle. Tick marks allow the correct setting of the angle in 15 ° intervals. A Thermocoax single-core heating element of 10 mm hot length and 1 mm diameter was used as heat source. It runs in a S-shape inside the heater block. A clamp holds the sample in place.

Figure 3.7 shows a drawing of the sample heater. All metal parts of the heating stage were made from an Al alloy (AlMgSi1), except for the heating element cover, the clamp and the screws, which were made from stainless steel (X5CrNi1810). No external controls for the adjustment of sample height and tilt angle were included into the heating stage. This ensured maximum stability, but all adjustments had to be made before the vacuum chamber is closed.

[1] Fabricated by CVM GmbH Chemnitz, Germany

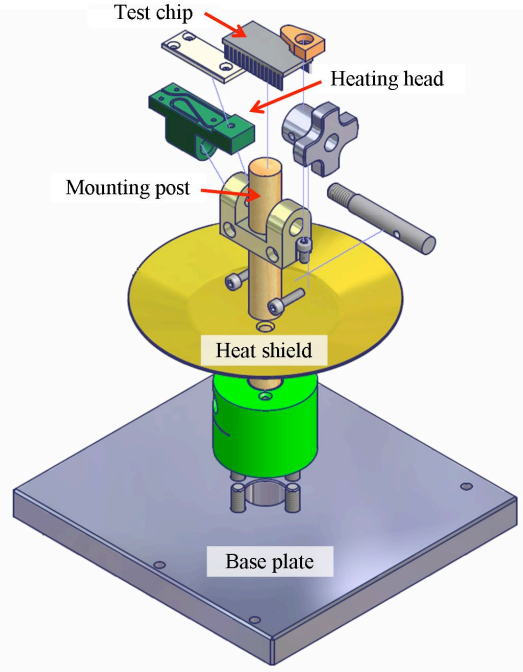


Fig. 3.7: Sample heating stage for the LEO Gemini 1550 SEM.

Regulation of heating current and sample temperature

Temperature variations during the *in-situ* EM experiments caused thermal expansion of the sample holder and led to mechanical sample drift. Consequently, the temperature of the specimen had to be kept as stable as possible. Additionally, a correct measurement of the temperature of the tested interconnect line is essential for the interpretation of the results. Hence, special attention was paid to this task for the experimental setup.

Due to the good thermal insulation of the specimen within the evacuated SEM chamber, only low electrical power had to be applied to the heating element in order to heat the sample to the desired temperature. However, the resistance of the used heating element is specified as 1.3 Ohms. Consequently, relatively high currents were necessary to achieve the desired temperatures. In this application the current ranged from 3 to 4 A for temperatures between 200 and 350 °C. These high currents cause a problem for the stability of the electron beam during imaging since relatively high electromagnetic fields are associated with them. The electron beam of a SEM is very sensitive to variations of the electromagnetic fields of the surroundings. Field fluctuations will result in image shifts and defocusing of the electron beam at the frequency of the

changes. Since active temperature control would involve undesired current regulation, no active temperature control system of any kind was used to avoid such field variations. Instead, a constant current was applied to the heating element. After a stabilization period of a few hours, a temperature stability better than 0.5 K per 10 minutes was observed. This stability was sufficiently stable for the software-based drift correction system to keep the sample area of interest within the field-of-view of the SEM at the desired magnification.

It was found that the current stability of the used power supply is an important quality criterion for this application. If too high, the residual ripple will cause jitter in the electron image at the mains frequency. The same problem occured if the individual electrical components did not share a common electrical ground potential. An Agilent E3632A DC power supply was used. It is specified with $< 2\,\mathrm{mA}_{rms}$ for Normal Mode Current and $< 1.5\,\mu\mathrm{A}_{rms}$ for Common Mode Current.

Two methods of monitoring the temperature of the sample were implemented in the setup. A thermocouple Newport HTMTSS-IM100G-150 was installed inside the vacuum chamber, and it was connected to a digital read-out. The tip of the thermocouple was firmly attached to the test chip package by the clamp of the heating head. It was used to monitor the temperature during an experiment visually. Simultaneously, the resistance of the test structure itself was used to correctly adjust the temperature to the desired value and to monitor and record it during the entire experiment time. In order to do this temperature-resistance curves of reference samples were recorded inside an oven. An offset between the thermocouple reading and the actual sample temperature obtained from the resistance measurements was found, due to the poor heat conduction between the ceramic package and the heating head.

Current stressing and resistance monitoring

A Keithley Model 2400 general-purpose SourceMeter® was used as current source for the EM experiments. It can simultaneously act as power supply and precisely measure the resistance of the connected structure. Two modes of operation are possible: constant current mode or constant voltage mode. Resistance measurements can be performed in 2- or 4-wire configuration. It can be remotely controlled through a GPIB-Interface [73].

The internal design of the bond pad connections of the test structures required that the sourcemeter was used in 2-wire configuration, since the second con-

nection to the cathode end of the interconnect line had to be cut during the sample preparation. The stressing current was supplied in constant current mode. For simple resistance measurements a current of 300 μA was applied to the sample, and for EM stressing the current was increased according to the experiment plan.

Electrical connections

The electrical connections for the additional components inside the SEM chamber such as sample heater, thermocouple and the sample itself were established using a 18-pin feedthrough vacuum flange. For the wiring inside the SEM chamber 0.8 mm transformer wire was used. This type of wire is coated with a relatively temperature resistant lacquer. After an adaption period, the evaporation of volatile components ceased and stable vacuum conditions were achieved. Clamps were used to connect the individual components inside the SEM chamber. Standard laboratory cables were used for all other connections outside the electron microscope. A simplified wiring diagram is given in figure 3.8.

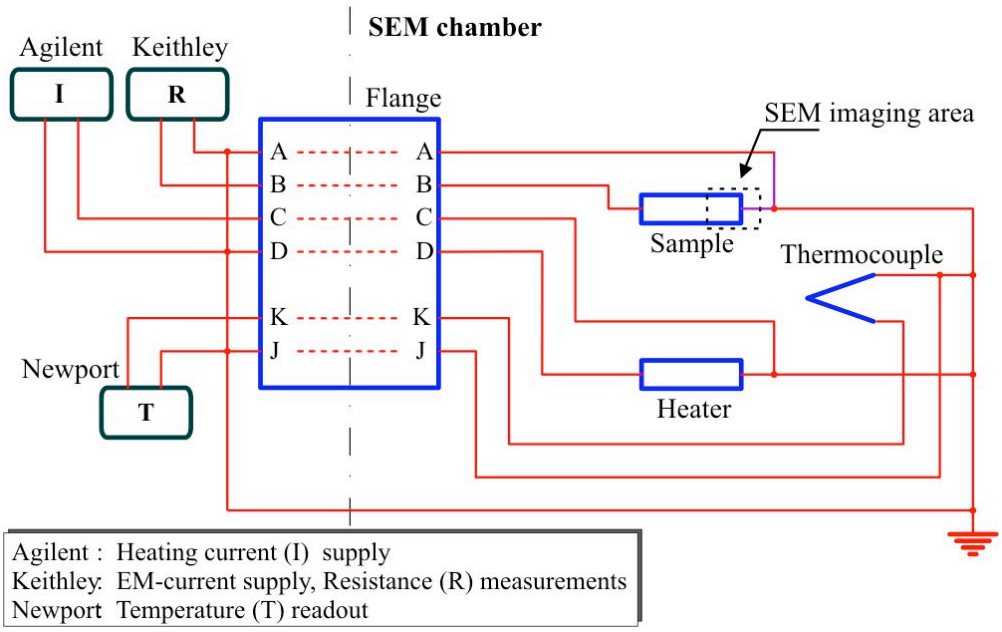


Fig. 3.8: Wiring diagram of the experimental setup including heater connection, thermocouple, resistance monitoring and stressing current.

Sample drift correction

The sample heating stage exhibited a slow mechanical drift due to temperature variations. This drift required additional measures and corrections in order to maintain the sample position under the electron beam during an experiment. For this purpose, a remote control software (SEM Drift Control) for the LEO Gemini 1550 SEM was developed [74]. This software is capable to perform multiple tasks such as image recording to any location including network directories, detection of image shift, sample (re)positioning and auto focusing. The communication between the remote-control computer and the LEO Gemini 1550 SEM computer was realized via the serial port (RS232) interface. Together with the corresponding command library and in combination with the internal macro library of the SEM, this solution allows to remotely control all relevant functions of the SEM, such as:

- Reporting and setting SEM parameters:
  - stage position
  - beam position
  - detector settings
  - focus
- Setting of image acquisition parameters:
  - scan rate
  - noise reduction
  - freezing and saving of images
- Calling macros from the internal library

3.2.3 Information depth and resolution of *in-situ* SEM images

The image sequences that were acquired during the *in-situ* EM experiments contain information about the void sizes (two-dimensional projections) as well as their positions within the interconnect lines. However, due to the three-dimensional geometry of the samples, the interpretation of the *in-situ* SEM images is challenging. Considerations regarding the interaction volume of the primary electrons with the sample are necessary in order to estimate the minimum detectable void size as well as the maximum depth of detection. Voids can occur in a depth of about 100–500 nm below the FIB cross-section, depending on the remaining passivation thickness in front of the interconnect line and the actual position of the voids within the line itself. In this depth,

the excitation volume of the electron beam is already relatively large. Hence, the volume of origin of the secondary electrons that contribute to a pixel of the SE images is increased. Moreover, at a primary electron energy of 20 keV, their penetration depth is limited.

Monte-Carlo simulations were performed in order to evaluate the penetration depth of the primary electrons for a tilt angle between the FIB cross-section and the electron beam of 70 °. *In-situ* SEM imaging was generally performed at this angle. The simulations were carried out for a vertical position on the FIB cross-section of 50 % of the line height. Figure 3.9 shows a drawing of the sample geometry together with the Monte-Carlo simulation results.

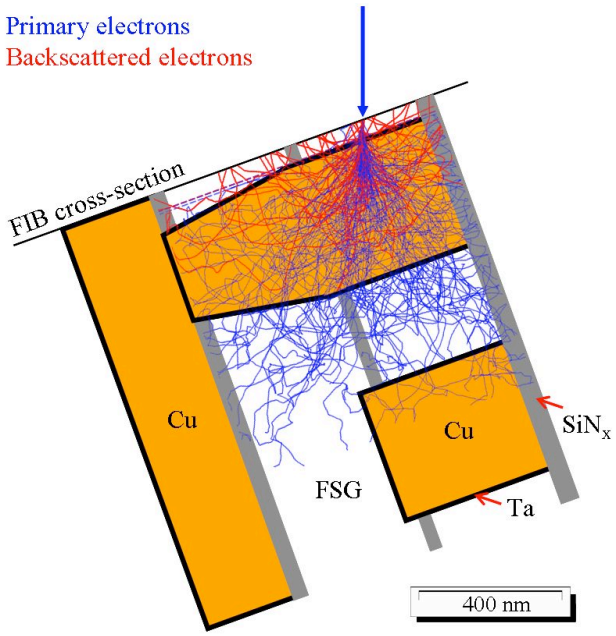
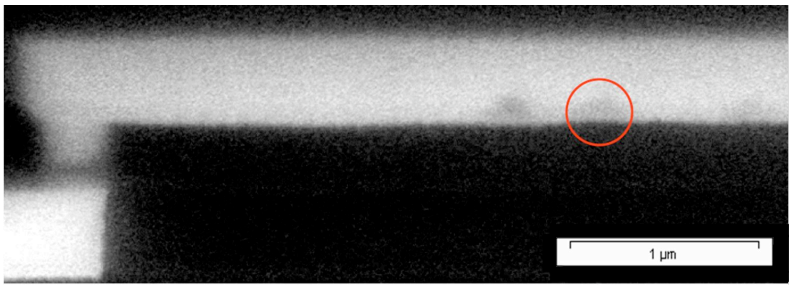


Fig. 3.9: Monte-Carlo simulation of electron trajectories in *in-situ* SEM samples.

The majority of the primary electrons penetrates up to about 200 nm below the Ta barrier at the sidewall of the line. As a result, mainly voids that exist within this region of the line can be detected. It is difficult to assess theoretically the limitations for the minimal detectable void size. The experiments demonstrated that voids as small as 50 nm in diameter can be detected near the bottom barrier interface of a CuAl sample. In figure 3.10, an *in-situ* SEM image is shown together with a TEM image of the same CuAl sample. The void in the marked region measures 50 nm in height.



(a) *In-situ* SEM image.

(b) TEM brightfield image

Fig. 3.10: *In-situ* SEM image and TEM image of a stressed CuAl sample. The void within the circle measures 50 nm.

Chapter 4

Case studies of electromigration

4.1 *In-situ* SEM investigations

In this section, the EM-induced degradation phenomena that were observed during the *in-situ* EM experiments on individual samples will be described. The time-resolved formation, propagation and growth of voids will be correlated to the results of post-mortem EBSD analyses in order to investigate the influence of the local microstructure. For all discussions in this section, the direction of the electron current is upwards through the via and then along the upper metal line as indicated in the *in-situ* SEM image sequences. The material transport occurs in the same direction while the voids move virtually in the opposite direction. The EM-induced degradation of the interconnects will be generally discussed in terms of void movement rather than atom movement, even knowing that the atomic transport is the real EM-induced solid-state physical process, and that the void movement is only a visualization of this process. In each image sequence, several positions were marked, and their relative distance from the end of the stressed metal line is given in the text.

4.1.1 Experimental conditions

Table 4.1 provides an overview of the stressing conditions used during the *in-situ* SEM investigations. T is the temperature of the samples before the high stressing current was applied. I is the absolute stressing current and j the current density in the line under test. The difference in j between Cu and CuAl samples for the same absolute current results from the slightly different cross-section areas. t_{Image} is the imaging interval from the *in-situ* experiments.

It consists of a user defined delay time plus the time required for sample repositioning and image capture.

Table 4.1: Experimental conditions for *in-situ* EM experiments.

Sample	T [°**C**]	I [**mA**]	j [**MA/cm**^{2}]	t_{Image} [**sec.**]
Cu-sample 1	150	15	12.5	90
Cu-sample 2	210	30	21	30
Cu-sample 3	218	30	21	35
Cu-sample 4	230	30	21	35
CuAl-sample 1	200	20	12	140
CuAl-sample 2	200	30	17.5	330
CuAl-sample 3	272	30	17.5	120
CuAl-sample 4	228	30	17.5	90
Cu/CoWP-sample 1	310	15	15	45
Cu/CoWP-sample 2	345	10	10	175

The high currents applied during the *in-situ* EM experiments resulted in a significant amount of Joule heating. In order to quantify the temperature increase due to Joule heating and to correct the actual test temperatures accordingly, the resistance of the EM test structures was measured at two different current settings, 0.3 mA and 30 mA respectively. At a current of 0.3 mA, Joule heating can be neglected. A current of 30 mA was typically used as stressing current during the *in-situ* EM experiments. The resistance of the interconnects was increased compared to the low-current measurement. The following equation was used to calculate the Joule heating-induced temperature difference:

$$\Delta T_{Joule} = \frac{\Delta R_{Joule}}{R_{0.3} \cdot TCR} \tag{4.1}$$

In this case, ΔT_{Joule} is the temperature difference due to Joule heating, ΔR_{Joule} the corresponding resistance difference and $R_{0.3}$ the resistance at 0.3 mA measurement current. TCR is the temperature coefficient of the resistivity.

Table 4.2 lists the temperature differences due to Joule heating together with the resulting overall test temperatures. The Joule heating contribution (ΔT_{Joule}) to the sample temperature amounts to an increase of 60-70 K. The resulting overall test temperatures T_{EM} were in the same range as for the standard accelerated lifetime tests.

Table 4.2: Joule heating contribution to the sample temperature during *in-situ* EM experiments.

Sample	j **[MA/cm^2]**	ΔT_{Joule} **[K]**	T_{EM} **[°C]**
Cu-sample 3	21	65	283
Cu-sample 4	21	63	293
CuAl-sample 3	17.5	67	339
CuAl-sample 4	17.5	62	290

4.1.2 EM in Cu interconnects

Cu-sample 1

Interconnect degradation vs. time Figure 4.1 shows an *in-situ* SEM image sequence of the cathode region of Cu-sample 1. The initial void formation occurred after about 4 hours at several locations along the capping layer interface of the line some μm away from the via. Shortly after this, a void appeared directly above the via. Over the course of the experiment, the line voids slowly moved towards the line end and merged into the via void. The via void grew and began to extend into the via. This process appeared to be discontinuous as several jumps in the via size could be observed at particular times during the experiement. However, the time scale of these jumps is in the order of several tens of minutes, which means that the responsible material transport mechanisms are still relatively slow processes. Towards the end of the experiment, the size of the void at the line end decreased again significantly. Clearly, a redeposition of material from the via to the line end above it took place. The experiment was stopped after 55 hours. It is interesting to note, that the overall resistance increase of the test structure at the end of the experiment was less than 2 % of the initial resistance. The very long lifetime of this sample can be explained by a significantly lower temperature and current density compared to the other experiments. Additionally, it has to be considered, that this sample is a M2M1 test structure from a 180 nm technology wafer, instead of a M5M4 test structure of a 130 nm wafer like the other samples.

Interconnect degradation vs. microstructure Several changes in the void growth rate were observed on this sample as the void extended into the cathode via. In order to investigate the root cause for this behavior, the morphology of the inner void surface was studied. A FIB cross-section was prepared perpendicular to the original imaging plane. The original imaging cross-section had been covered with FIB-deposited platinum in order to protect it before the new cross-section was cut into the center of the via. Figure 4.2 shows an overview image of the sample after preparation of the second cross-section (a) as well as a close-up image of it (b). In this image the current direction is upwards through the via and into the page. The FIB-cut confirms that the remaining passivation thickness on the original imaging plane was in the range of 100 nm. Furthermore, all relevant interfaces of the test structure remained intact over the course of the experiment. No grain boundaries are visible in the redeposited material in the upper part of the

via. The parallel lines that run diagonally across the lower part of the via represent former grain boundaries. It is likely that they originally formed the boundaries of a narrow recrystallization twin. This microstructure is assumed to be the reason for the observed discontinuities in the void growth rate.

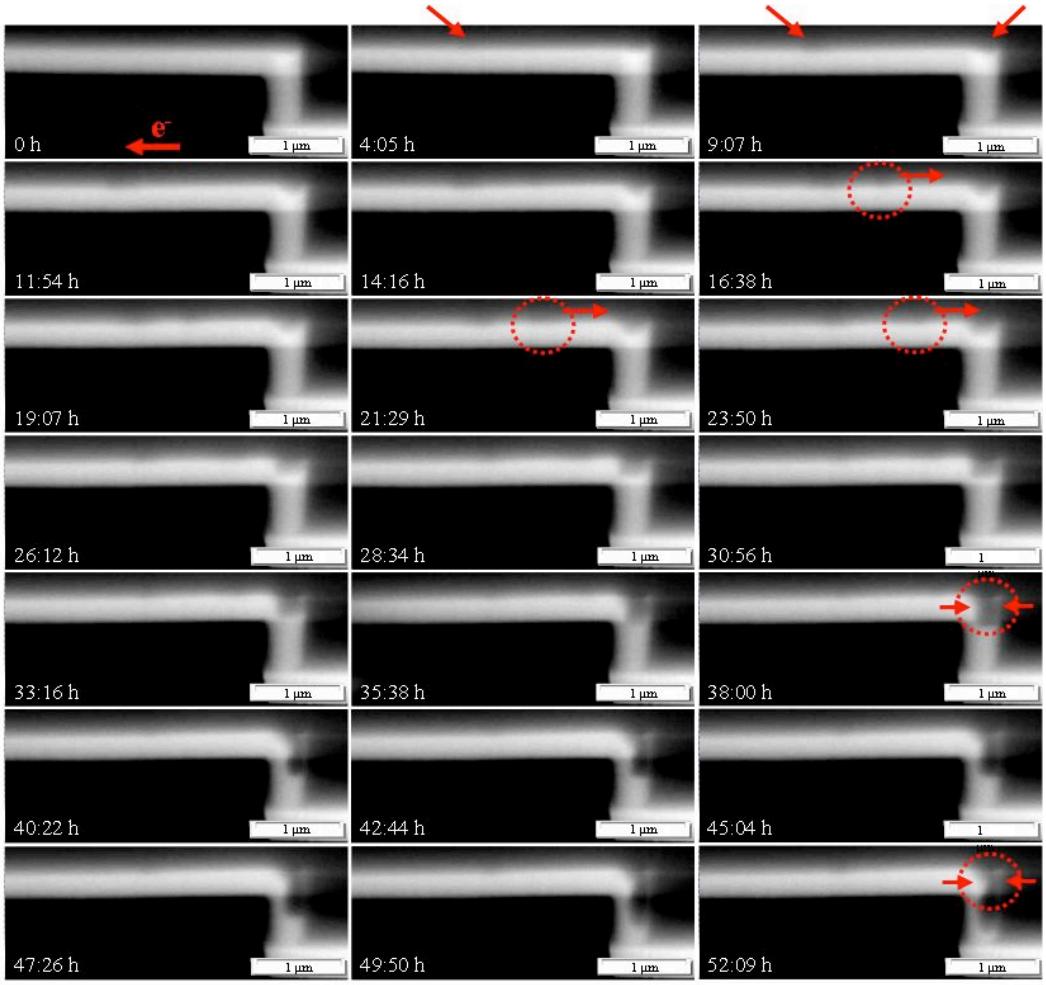
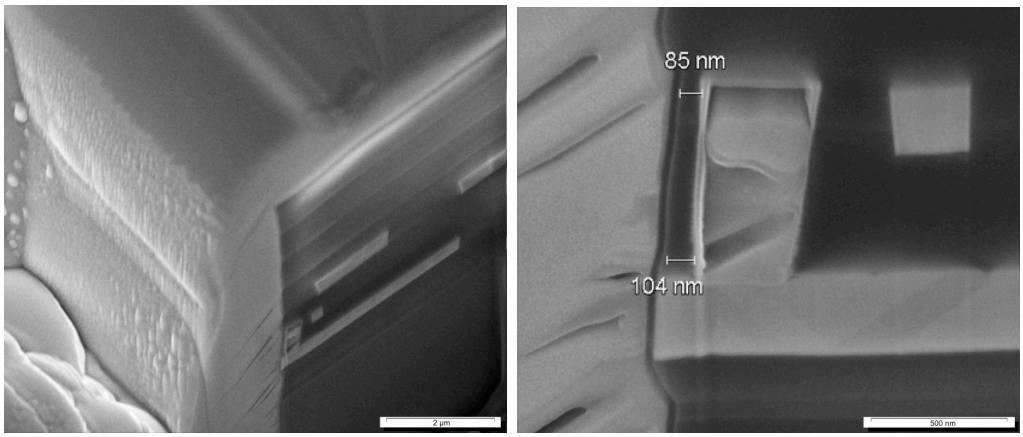


Fig. 4.1: *In-situ* SEM image sequence for Cu-sample 1.



(a) Overview image after FIB preparation. (b) Close-up image of the cathode via.

Fig. 4.2: Post-mortem SEM/FIB analysis of Cu-sample 1.

Cu-sample 2

Interconnect degradation vs. time Figure 4.3 shows an *in-situ* SEM image sequence of the cathode region of Cu-sample 2. In this sample, the first voids appeared after about 15 minutes at the Cu/capping layer interface simultaneously at two positions along the line, at position A (0.5 μm away from the line end) and at position B (2.2 μm away from the line end). Both voids remained fixed at their positions for some time. After 50 minutes, another void appeared moving into the field-of-view from the right side (position C, 3.5 μm away from the line end). It became trapped at this position and did not move further. Towards the end of the experiment, this void continued to grow again. Immediately after the void had appeared at position C, the void at position B started to move along the line towards the via. It experienced a number of shape and speed changes and finally merged into the void at position A. The period of time the void needed in order to move from position B to position A was approximately 25 minutes. The combined void immediately continued to move towards the line end and began to grow and eventually extended down into the via. Subsequently, at least one additional void appeared at position C and moved towards the via, merging into the large via void. The large void at the via underwent several shape changes as it grew into the via. Again, a redeposition of material into the upper region of the via could be evidenced. The sample failed due to the via void after 3:15 hours.

Interconnect degradation vs. microstructure The EM-video of this sample revealed several sites of particular interest (A–C in figure 4.3). Positions A and B were identified as void nucleation sites. Especially at position B, continuous void formation was observed. In contrast to that, position C acted as a trapping site for voids as they moved towards the cathode end of the test structure. Furthermore, significant material redeposition was observed at the line end above the via. In order to investigate the local microstructure around these positions an EBSD analysis was performed on the cross-section after the EM experiment was completed. For this, the remaining passivation was removed from the cross-section by using FIB. Figure 4.4 provides a SEM image of the cross-section of Cu-sample 2 together with an inverse pole figure (IPF) map showing the crystallographic orientation of the individual grains relative to the wafer surface. The void nucleation site B is located above a cluster of small grains. On both sides of this position, the cathode side on the left and the anode side on the right, the microstructure is dominated by large grains that extent across the entire height of the line (bamboo-like structure).

Similarly, the microstructure at position C is dominated by a cluster of small grains above which the void was trapped. Again, this cluster is surrounded by regions of bamboo-like microstructure. At the cathode side of the cluster (left), a twinned region can be seen. It consist of four grains colored in green and cyan. The grain-to-grain misorientation of 60 ° and the periodic arrangement of the grains is characteristic for recrystallization twins in fcc-materials. The microstructure of the via at the end of the interconnect line is dominated by a single large grain. No additional grain boundaries were observed in the region where the redeposition of material was observed during the final stages of the *in-situ* EM experiment.

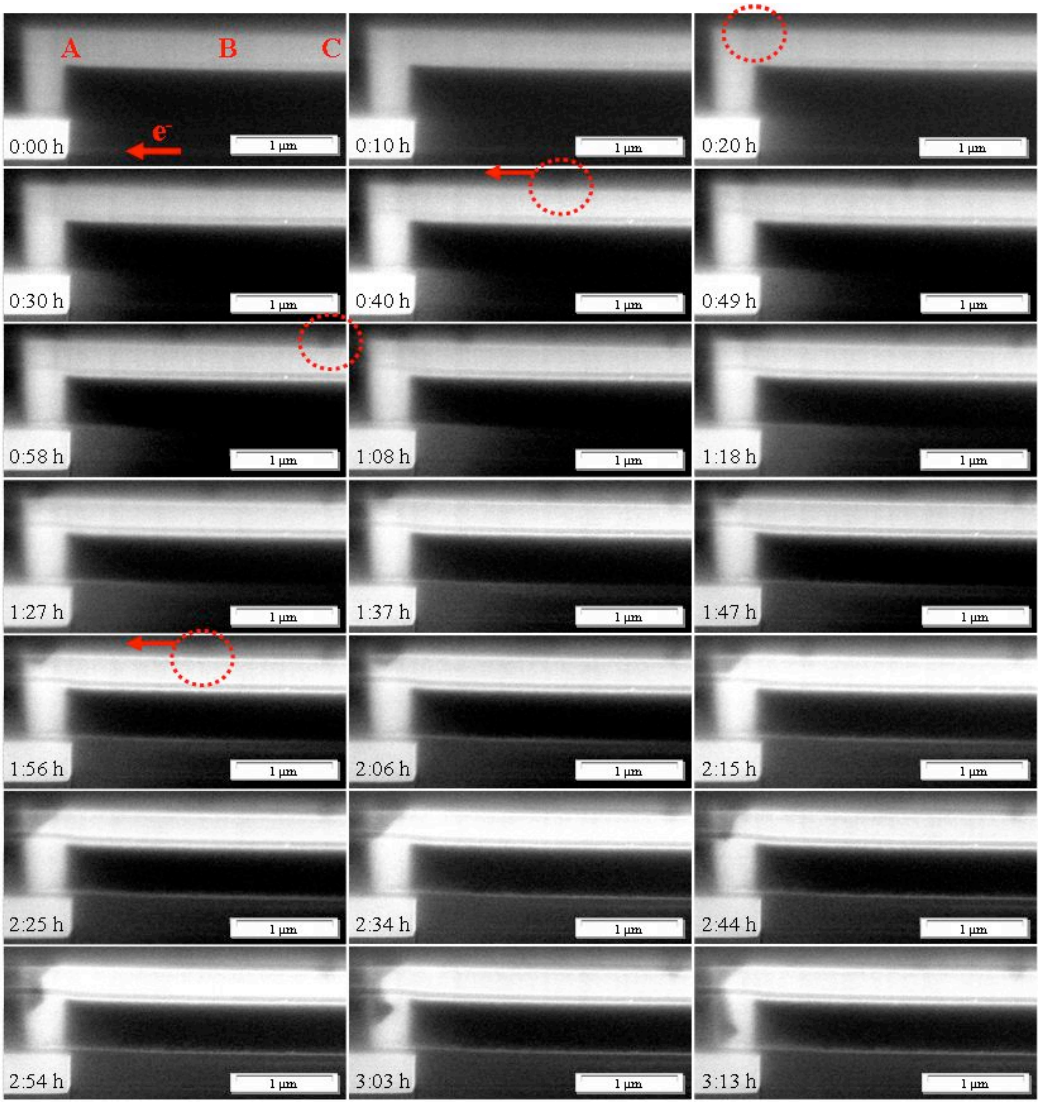
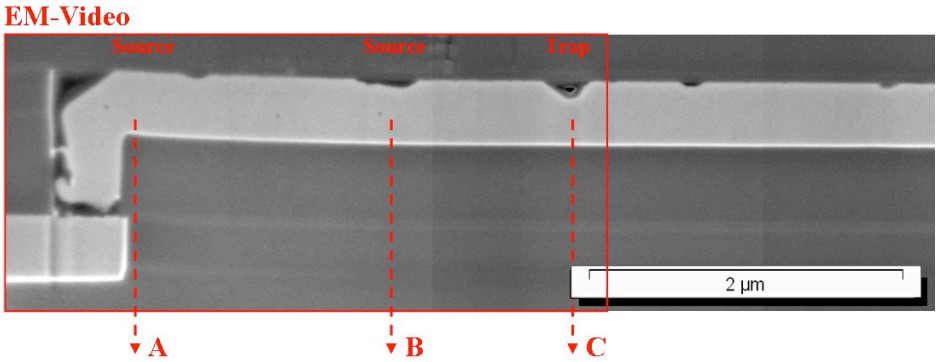
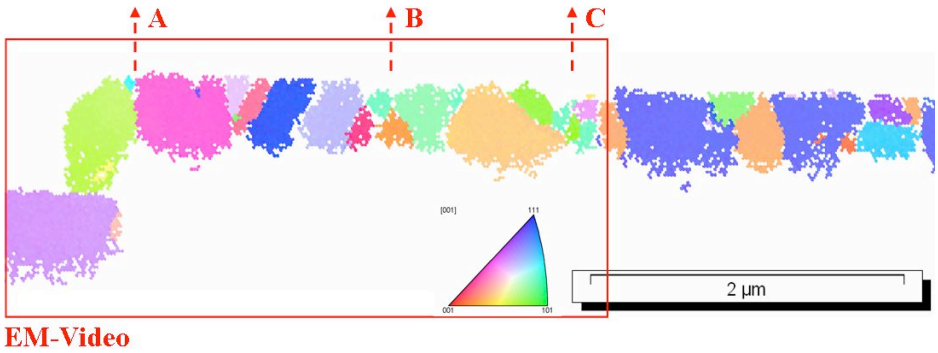


Fig. 4.3: *In-situ* SEM image sequence for Cu-sample 2.



(a) SEM image of the cathode region.



(b) Inverse pole figure (IPF) map.

Fig. 4.4: Post-mortem SEM/EBSD analysis of Cu-sample 2.

Cu-sample 3

Interconnect degradation vs. time Figure 4.5 shows an *in-situ* SEM image sequence of the cathode region of Cu-sample 3. As for the previously described samples the void formation occurred at the Cu/capping layer interface. After 10 minutes the first void appeared several micrometers away from the line end (position A, 2.5 μm away from the line end). From there, the void began to move relatively fast towards position B (1.3 μm away from the line end, period of time 16 minutes). On the way towards position B, the void experienced several shape and speed changes. On one occasion, it was divided into two voids. A smaller void followed the larger one for some time, but both remerged into one void before reaching position B. There it became trapped and remained stationary for a relatively long period of time (28 minutes). Then, another void was formed at the line end directly above the via and started to grow slowly. After 35 minutes of total experiment time, more voids appeared near position A and moved fast towards position B, merging there into the already existing void. Finally, after 54 minutes, the void at position B began to move again. With some shape changes, it moved slowly towards the line end, thereby stopping briefly at position C (0.75 μm away from the line end). After 76 minutes, all voids had merged into the void at the line end. This void then continued to grow in size and to extend into the via. Again, material redeposition into the line end region occurred. The sample failed due to the via void after 2:56 hours.

Interconnect degradation vs. microstructure Two particular sites of interest (positions A and B in figure 4.5) were identified on this sample. The void nucleation occurred mainly at position A, and then, the voids propagated quickly towards position B, where they became trapped for a long period of time. The void propagation speed between position B and the line end was found to be much lower and associated with several stops compared to the region between the positions A and B. The EBSD analysis of this sample, shown in figure 4.6, revealed, that there are only <111>-oriented grains (blue) present in the segment between positions A and B. This highly textured <111>-region extends even beyond position A on the anode side (left in image). On the cathode side of position B (right in image), a <511>-oriented grain (pink color) was found. Such grains are known to represent coherent twin grains to neighboring <111>-oriented grains. From position B towards the line end such <511>-oriented grains are repeatedly found alternating with <111>-oriented grains. One of the <511>-oriented grains is located at position C, where the void had briefly stopped on its way toward the line end. It

is worth to note that no voids or signs of delamination were detected along the Cu/capping layer interface in the post-mortem SEM/EBSD analysis. All voids were completely refilled during the EM-experiment.

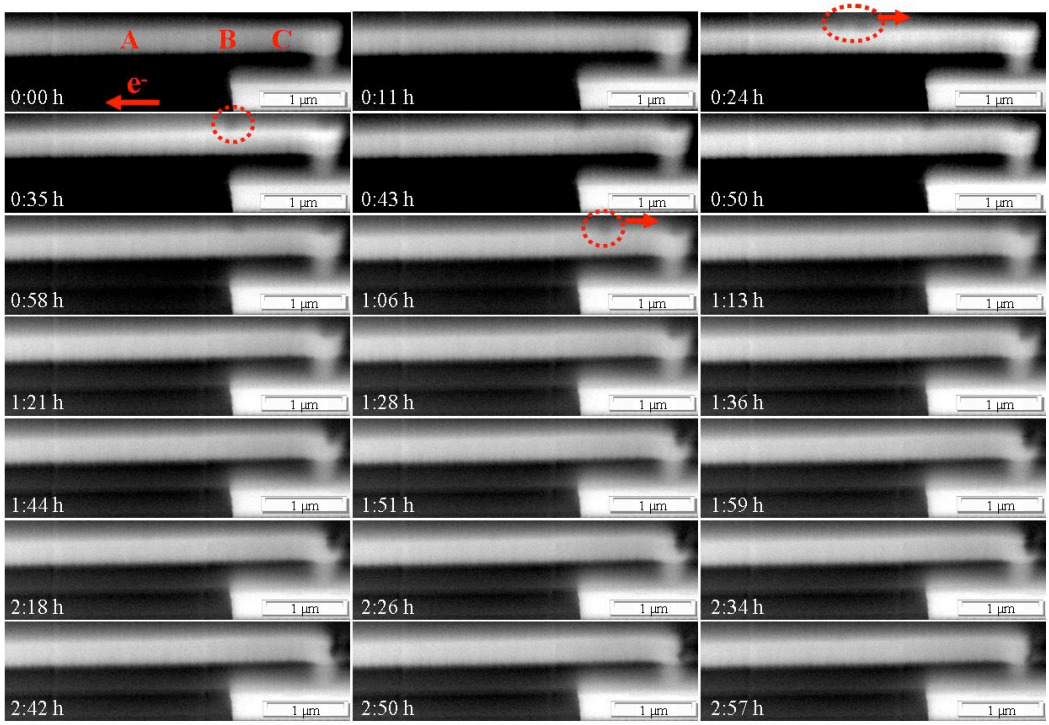
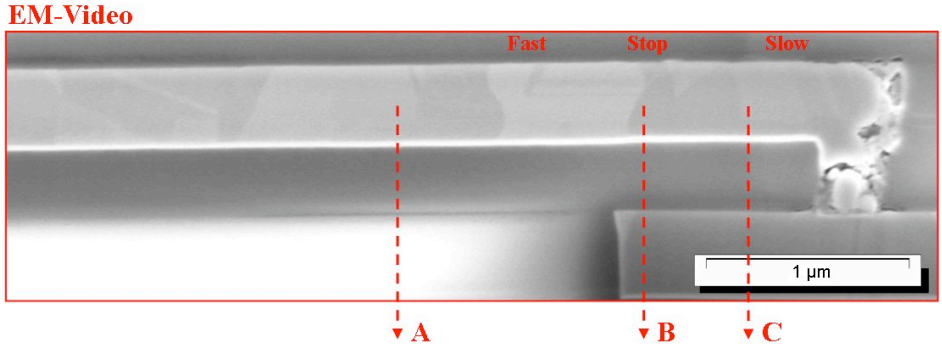
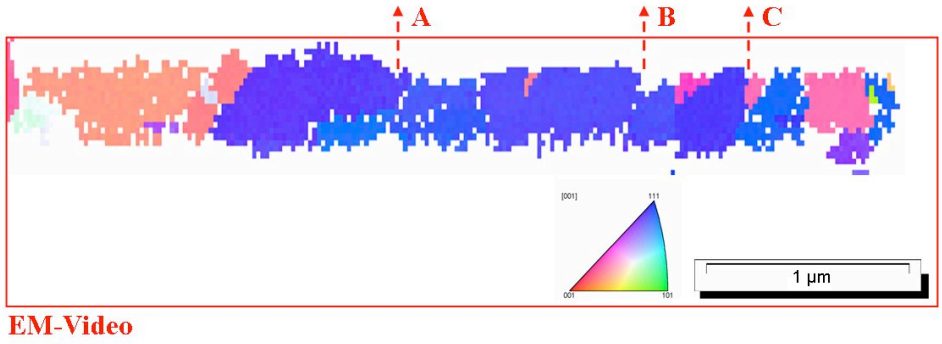


Fig. 4.5: *In-situ* SEM image sequence for Cu-sample 3.



(a) SEM image of the cathode region.



(b) Inverse pole figure (IPF) maps.

Fig. 4.6: Post-mortem SEM/EBSD analysis of Cu-sample 3.

Cu-sample 4

Interconnect degradation vs. time Figure 4.7 shows an *in-situ* SEM image sequence of the cathode region of Cu-sample 4. The first voids became visible after 31 minutes simultaneously at two positions along the Cu/capping layer interface, about 2.1 μm away from the line end (position A) and directly at the line end above the via. The void at the line end began to grow relatively slowly. After 68 minutes a part of the void at position A detached from the rest and began to move very slowly towards the line end. It uniformly grew at the same time. It is important to note, that its shape did not change significantly while moving. The remaining void at position A stayed there until the end of the experiment. During the entire time, the void above the via continuously grew and the sample eventually failed after 2:55 hours due to the via void (before the other voids reached the line end). The voids were preserved at position A and position B (1.1 μm away from the line end), respectively.

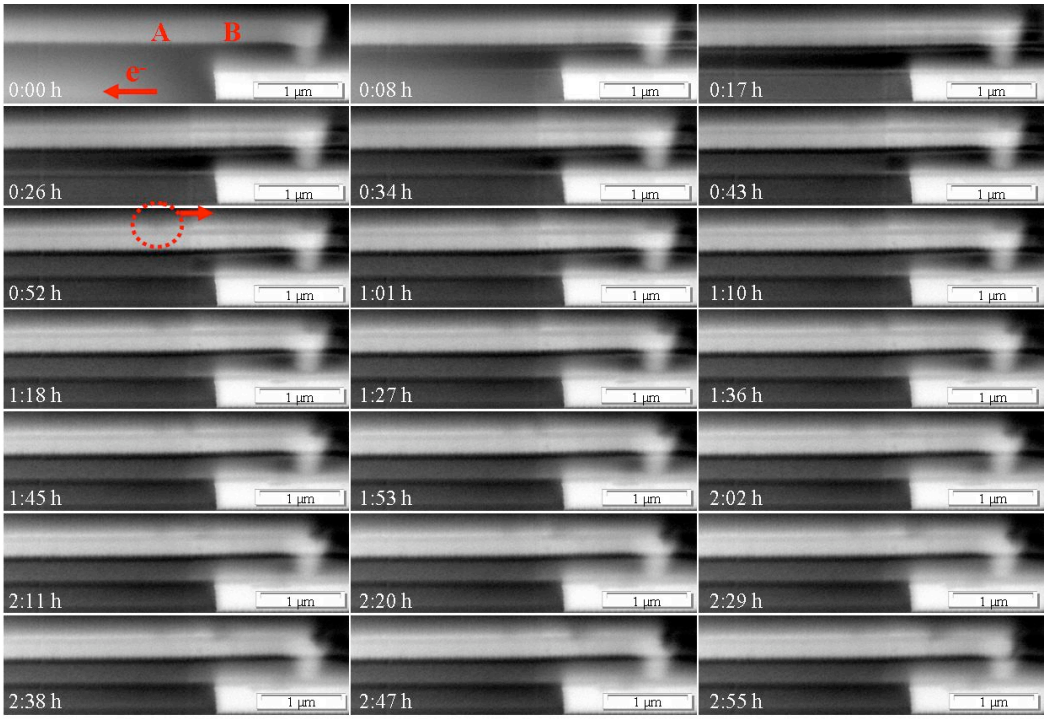
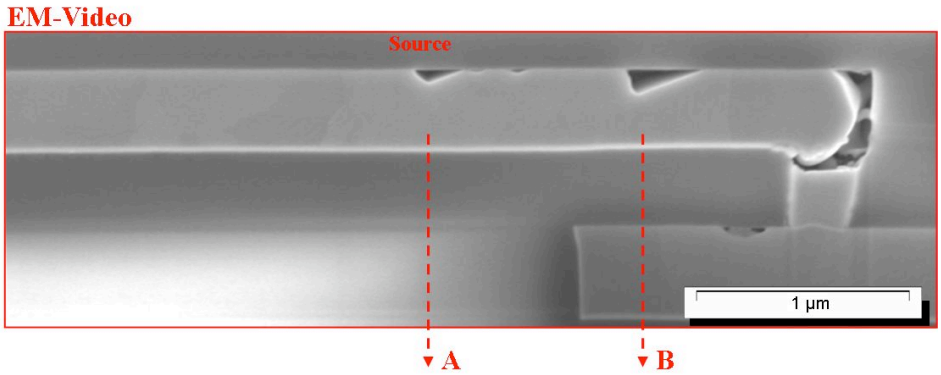
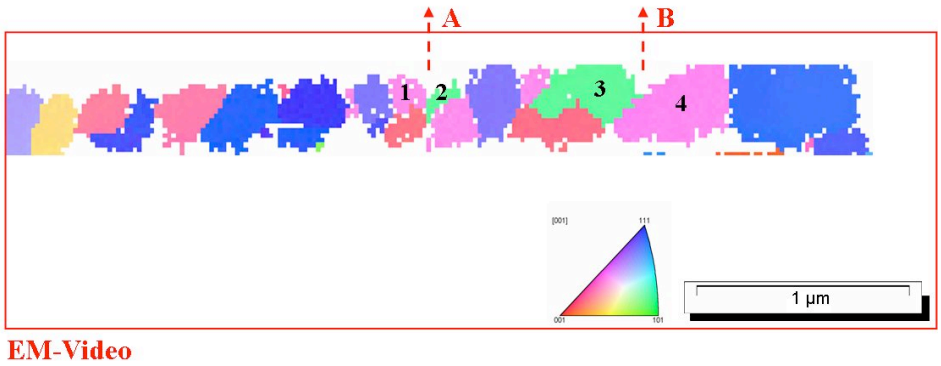


Fig. 4.7: *In-situ* SEM image sequence for Cu-sample 4.

Interconnect degradation vs. microstructure As explained above, the positions of the voids in this sample were preserved during their movement along the Cu/capping layer interface when the sample failed. Thus, this sample represents a unique opportunity to analyze the material transport mechanisms across the free Cu surfaces of the voids as it takes place. Figure 4.8 provides the SEM image of the FIB cross-section and the corresponding IPF map as obtained in the post-mortem EBSD analysis. Two voids are visible with similar shapes, one above the grains marked as 1 and 2, and the second one above the grains marked as 3 and 4. These two voids correspond to positions A and B marked in figure 4.7, respectively. Both voids exhibit the same inclination angle of the free surface on the cathode side (right) of the void. However, the angle of the free surface on the anode side (left) of the void is different. The grains that provide the free Cu surfaces have similar orientations for both voids, except that their relative positions to each other are swapped. Some conclusion regarding the void shapes can be drawn from the *in-situ* SEM video. The void at position B traveled across grain 3 without shape changes. Hence, both void surfaces are correlated to lattice planes in this grain. Since the void at position A did not travel, it is unknown which of the adjacent grains controlled the formation of the inner surface. From the angle of the cathode side surface of the void it is assumed that this surface is determined by grain 2, since it is the same angle as for the void in position B. The anode angle is assumed to be controlled by grain 1, since it does not match the angle measured on position B.



(a) SEM image of the cathode region.



(b) Inverse pole figure (IPF) maps.

Fig. 4.8: Post-mortem SEM/EBSD analysis of Cu-sample 4.

4.1.3 EM in CuAl interconnects

CuAl-sample 1

Interconnect degradation vs. time Figure 4.9 shows an *in-situ* SEM image sequence of the cathode region of CuAl-sample 1. In this sample, the first signs of void formation were seen after about 70 hours of experiment. An initial void appeared at the bottom Cu/barrier interface of the interconnect line at position A (3.2 μm away from the line end). Then, a part of the void detached from it and began to move relatively fast along the bottom Cu/barrier interface towards position B (2.5 μm away from the line end). There it disappeared briefly. By that time, a second void detached from position A and followed the first one along the bottom Cu/barrier interface. It moves slower than the first void and did not reach position B. Instead, it stopped earlier at position C (2.7 μm away from the line end). At the same time, the void at position B reappeared and continued to move slightly further to position D (2.3 μm away from the line end). After this, all voids remained inactive, except for some minor increase in their sizes. The entire void formation process lasted for about 4:30 hours. Subsequently, period of inactivity lasted for another 16 hours, before a new void appeared at the bottom Cu/barrier interface near position E (0.8 μm away from the line end). It moved along the bottom Cu/barrier interface around the corner into the via bottom. However, the via failed not immediately due to this void. The void continued to grow very slowly for another 18 hours before the sample finally failed after 108 hours of total experiment time. Hence, the entire void evolution process occurred within 38 hours, but it started only after 70 hours of EM stressing.

Interconnect degradation vs. microstructure The EBSD analysis of this sample revealed extended regions of a bamboo-like microstructure. The grains are generally larger compared to the Cu samples. This confirms the observations from the top-down EBSD analysis of unstressed reference samples (see section 4.3.3). As highlighted in figure 4.10, the voids are mainly located at junctions between a grain boundary and the Cu/barrier interface at the bottom of the interconnect line.

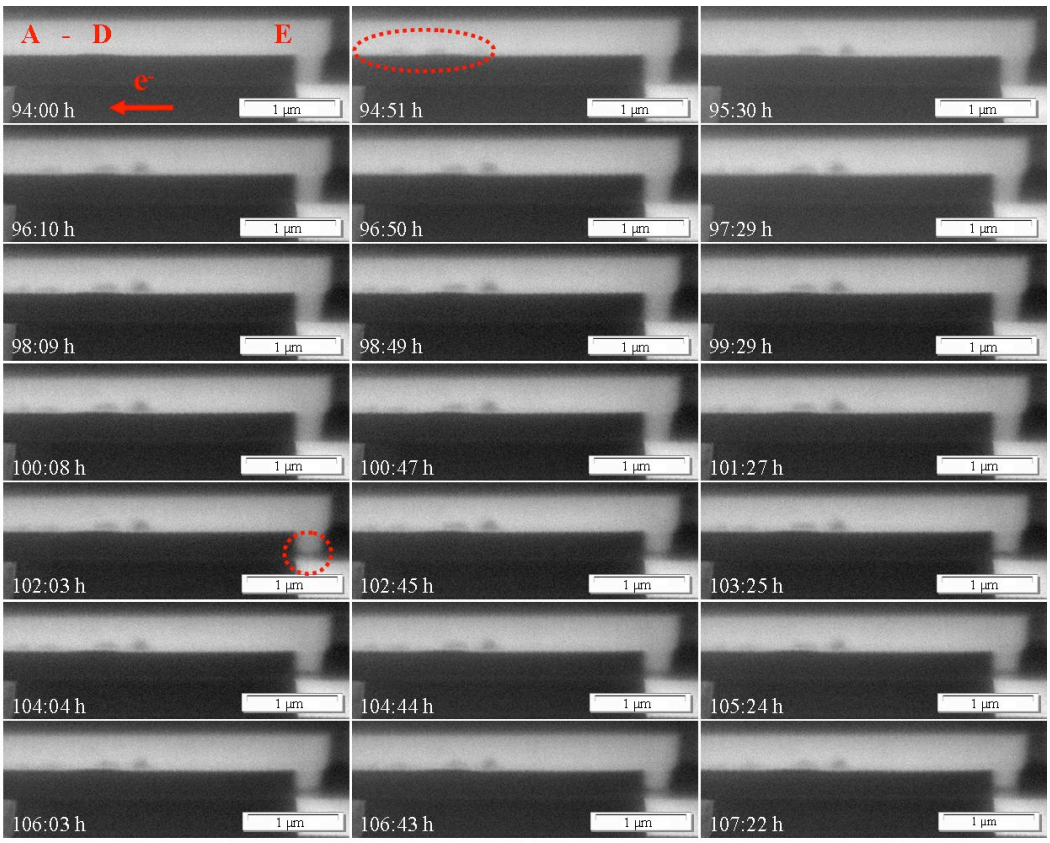
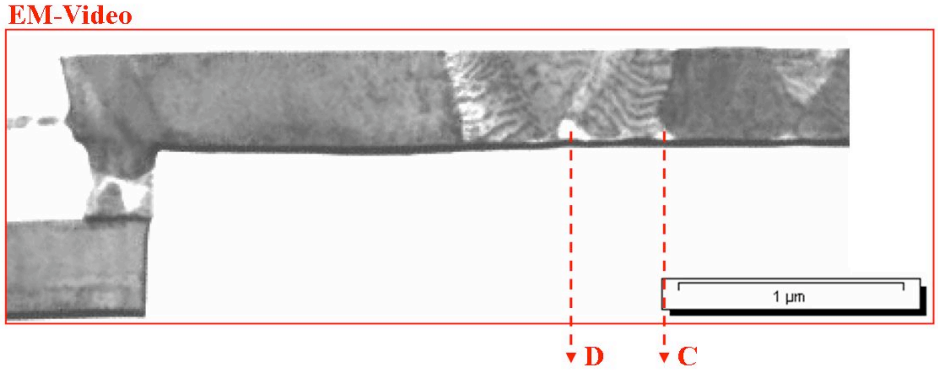
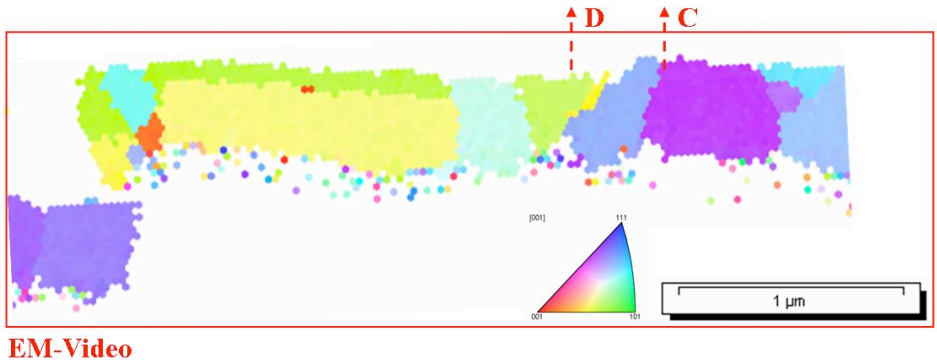


Fig. 4.9: *In-situ* SEM image sequence for CuAl-sample 1.



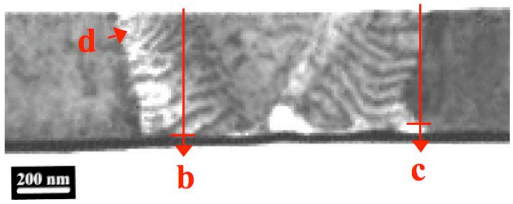
(a) TEM brightfield image of the cathode region.



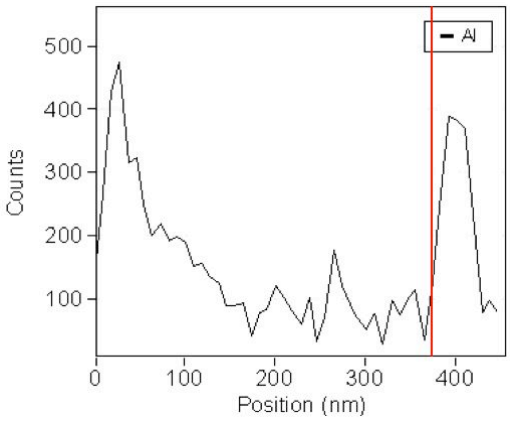
(b) Inverse pole figure (IPF) maps.

Fig. 4.10: Post-mortem SEM/EBSD analysis of CuAl-sample 1 (measured on TEM lamella).

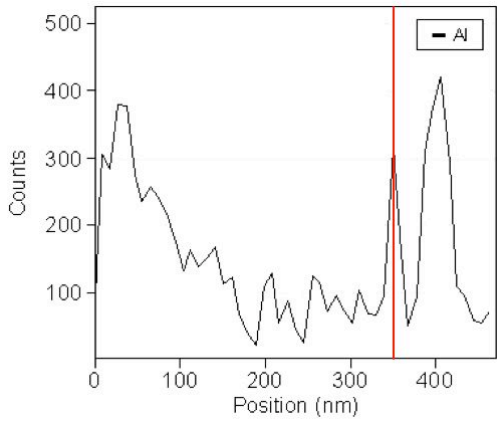
Spatial distribution of Al after EM-stressing This sample was used to study both, the spatial distribution of Al across the interconnect line as well as the local microstructure after EM-stressing. To do this, the cathode region of the interconnect line was extracted from the sample using a lift-out sample preparation technique [75]. Then, a TEM-lamella was prepared using FIB, and subsequently it was used for both analyses. The microstructure analysis will be described in the next section. The TEM/EDS analysis was performed prior to the SEM/EBSD investigation since beam damage is often associated with the SEM analysis of very thin TEM samples. Several EDS line scans were acquired in the vicinity of the voids at positions A–D (see above). Figure 4.11 provides the corresponding results. Three different line scans were acquired: across an undamaged region of the line (b), across a voided region (c) and across a grain boundary (d). It can be seen from the images, that the Al enrichment at the Cu/capping layer interface is still present. There is an Al gradient from top to bottom visible in both line scans, (b) and (c). Furthermore, in line scan (c) a significant enrichment of Al was observed at the inner Cu surface of the void (marked with a red line). In line scan (d) the intensity of the Al signal remains constant across the grain boundary. The intensity is in the range of 250 counts, which is in agreement to the intensity observed in the other line scans for the corresponding height of the line. This result indicates that the Al enrichment at the grain boundaries that was measured on unstressed samples may no longer be present. The high Al intensities in the Ta barrier region of line scans (b) and (c) are not real. They are a measurement artifact due to a drastically increased background noise associated with the Ta signal.



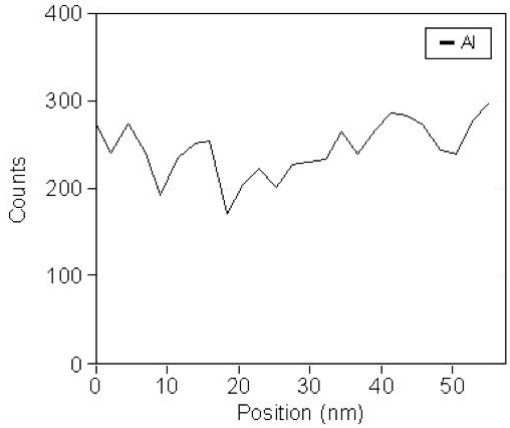
(a) Brightfield TEM image: overview.



(b) Line scan b.



(c) Line scan c.



(d) Line scan d.

Fig. 4.11: Spatial distribution of Al in CuAl-sample 1 after EM-stressing. TEM/EDS line scans across an undamaged region (b), a voided region (c) and across a grain boundary (d).

CuAl-sample 2

Interconnect degradation vs. time Figure 4.12 shows an *in-situ* SEM image sequence of the cathode region of CuAl-sample 2. During this experiment, the first void appeared at the Cu/capping layer interface. Its generation was not observed due to an experimental failure (loss of data for 10 hours between 65–75 hours of experiment time). After 75 hours, the void was first seen near the line end, where it remained inactive for the entire experiment and did not significantly contribute to the failure of the sample. After 78 hours of EM stressing, a void appeared moving relatively fast into the field-of-view, spanning across the entire visible height of the line. As it continued to move towards the line end, the top part of the void became trapped at the Cu/capping layer interface at position A (2.6 μm away from the line end), while the lower part continued to move along the Cu/barrier interface. Several significant shape and speed changes were observed before the void eventually dropped down into the via. It took about 3:20 hours from the first appearance of the void within the field-of-view until it reached the via. Another 2:40 hours later, the sample failed after the void had continued to grow further inside the via. This time corresponds to 84 hours of total experiment time. During the last 20 minutes of the experiment, the shape of the void at the top of the line end changed as well. Also, the remaining small void at the Cu/capping layer interface at position A disappeared during this period of time. This observation indicates material redeposition taking place in the line end region and along the capping layer interface during the final stages of the experiment before the sample failed.

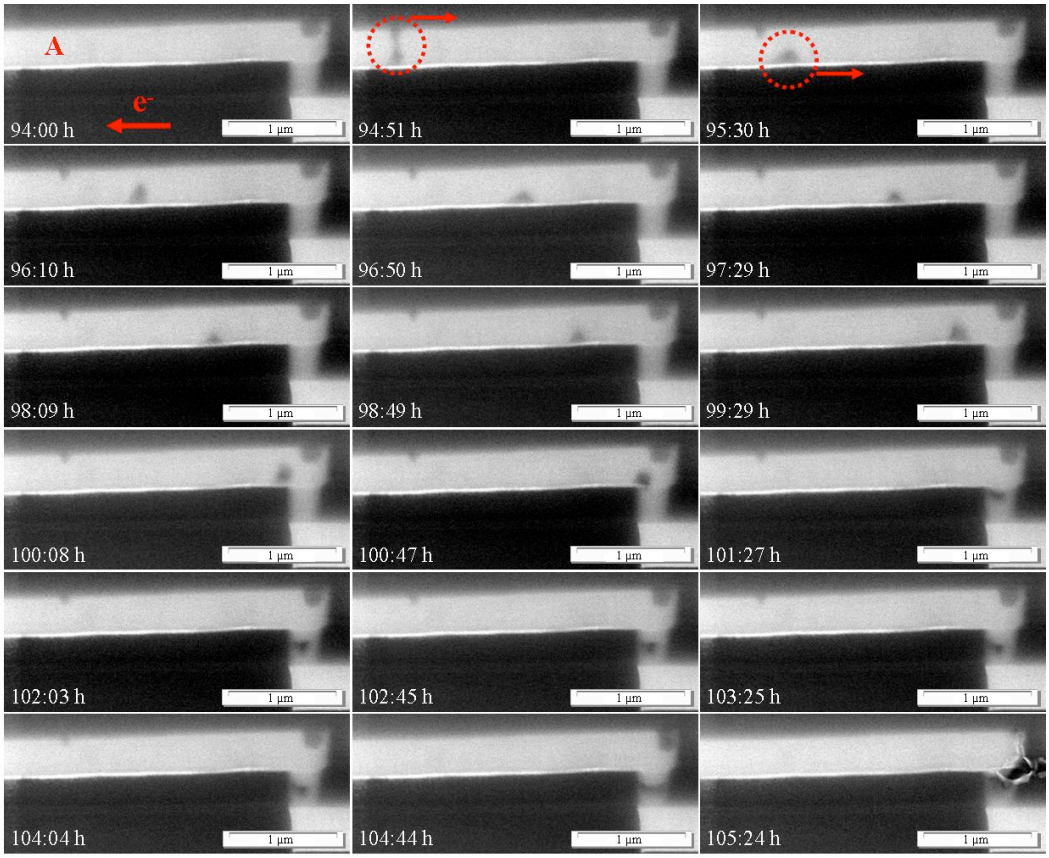


Fig. 4.12: *In-situ* SEM image sequence for CuAl-sample 2.

CuAl-sample 3

Interconnect degradation vs. time Figure 4.13 shows an *in-situ* SEM image sequence of the cathode region of CuAl-sample 3. During of the experiment, voids were formed at three positions along the Cu/capping layer interface of the interconnect line. The positions of these voids were almost equally spaced from each other. The first void appeared after 16 hours at position A (4 μm away from the line end). The second void appeared about 5 hours later at position B (2.7 μm away from the line end), and the third one appeared about 2 hours after that at position C (1.1 μm away from the line end). None of these voids moved away from their positions. Instead, they remained stationary. The voids at positions A and B grew to considerable sizes, while the void at position C remained relatively small. Moreover, large hillocks were formed directly adjacent to the individual void positions. This observation indicates that the diffusivity was very low along the Cu/capping layer interface of this sample. The sample failed after about 30 hours due to rapid void growth in the line during the final stages of the experiment, when the current density significantly increased due to the reduced cross-section of the line. It is important to note, that the failure mechanism observed on this sample was seen for a small fraction of all tested CuAl samples only. Moreover, it was observed only during a retest of additional samples two years after the wafers had been processed.

Interconnect degradation vs. microstructure This sample showed a significantly different degradation mechanism compared to the other CuAl samples. Instead of void generation and movement located at the Cu/barrier interface at the bottom of the interconnect lines, the degradation occurred at the top interface. Large stationary voids were formed at the top interface. The removed material piled up as hillocks directly adjacent to voids on the anode side. Due to the severe damage of the line, the interpretation of the EBSD results was very difficult, the IPF map does not necessarily show the original microstructure of the metal line. Nevertheless, the following conclusion can be drawn from the images in figure 4.14. The large hillock is composed of a twin-grain structure where a large Cu<111>-oriented grain (blue) is interspersed with Cu<511>-oriented twin grains (pink). This grain structure extends from the bottom of the line up to the top of the hillock. Furthermore, all neighboring grains show similar orientations. Near the undamaged via region, a void was found which resides on top of a Cu<111>-oriented grain (position C). Only Cu<511>-orientations could be measured within the highly damaged region to the right of the large hillock.

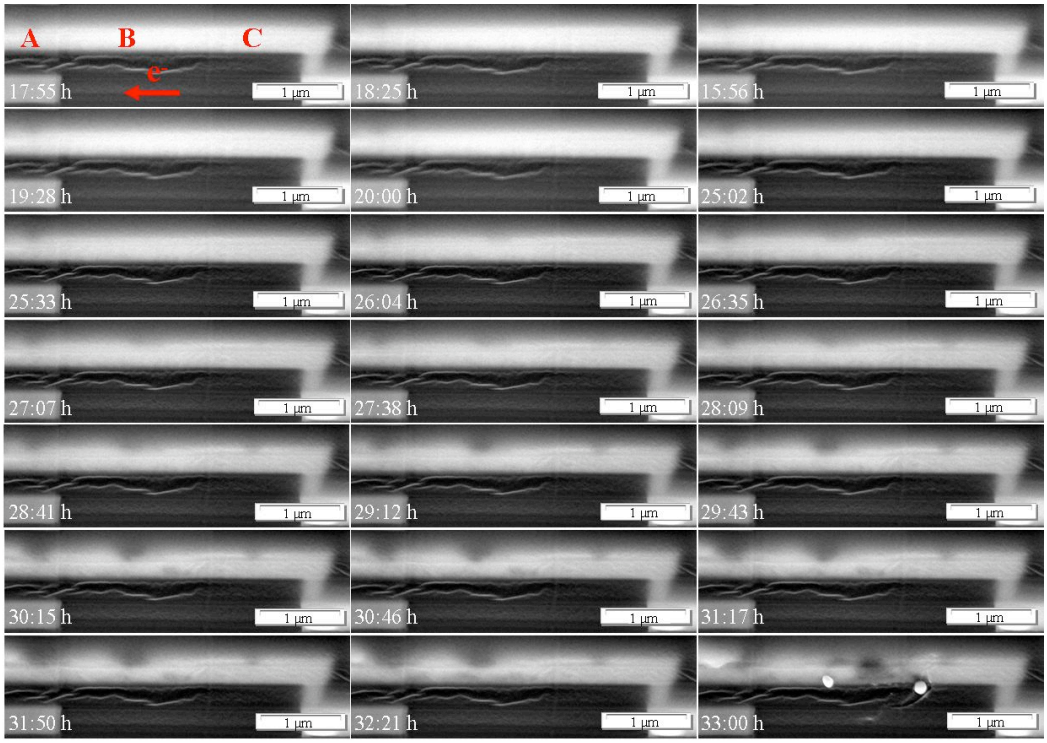
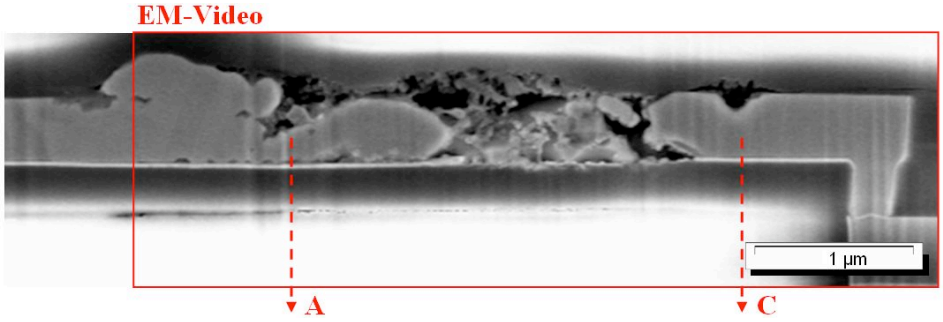
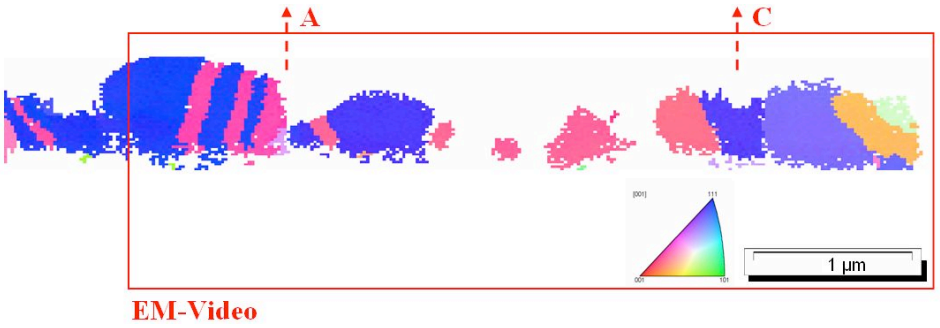


Fig. 4.13: *In-situ* SEM image sequence for CuAl-sample 3.



(a) SEM image of the cathode region.



(b) Inverse pole figure (IPF) maps.

Fig. 4.14: Post-mortem SEM/EBSD analysis of CuAl-sample 3.

CuAl-sample 4

Interconnect degradation vs. time Figure 4.15 shows an *in-situ* SEM image sequence of the cathode region of CuAl-sample 4. The first void was observed to move into the field-of-view along the Cu/barrier interface at the bottom of the Cu line after 33:30 hours. It remained barely visible until it reached position A (3.5 μm away from the line end). There it became more clearly visible. It continued to move further, and almost disappeared at position B (2.3 μm away from the line end). Shortly later, it reappeared at position C (1.9 μm away from the line end), where it stopped to move entirely. The time of travel from position A to C was only 1 hour. Subsequently, the void remained stationary until the experiment was stopped after a total time of 46 hours. The sample did not fail during this time. The repeated change in the visibility of the void on its way along the line is caused by a shift of the dominating material transport path from one interface of the interconnect to the other and back again depending on the position along the line.

Interconnect degradation vs. microstructure The failure mechanism observed on this sample involved once more the migration of a void along the Cu/barrier interface at the bottom of the Cu line. The correlation of the observations from the EM video to the post-mortem EBSD analysis results shown in figure 4.16 demonstrates that the void first appeared just left of the grain marked as 1. The predominant orientation in this region is Cu<111>, including grain 1 itself. From there, the void moved fast towards grain 3, where it became trapped, and it did not move any further. Interestingly, grain 3 exhibits an orientation close to Cu<511>. Just before the void reached grain 3, it almost disappeared in the EM video. The area correlates to the region between the grains 2 and 3. There, the IPF map shows several small grains with similar orientations. This observation could be an artifact due to the poor scan quality in this region, it could be either multiple grains or only one grain. Nevertheless, the void changed its path from near the frontside of the line towards the backside of the line as it passed this region. The FIB cross-section also reveals a small void at the Cu/capping layer interface at position C. This voids was not visible in the *in-situ* SEM video. Furthermore, narrow slit-like voids can be seen near the line end at the top interface. They extent vertically into the line perpendicular to the current direction along grain boundaries between grains 4 and 5 as well as 6 and 7. A relatively large void is also visible above the via. These voids were also not visible in the EM video.

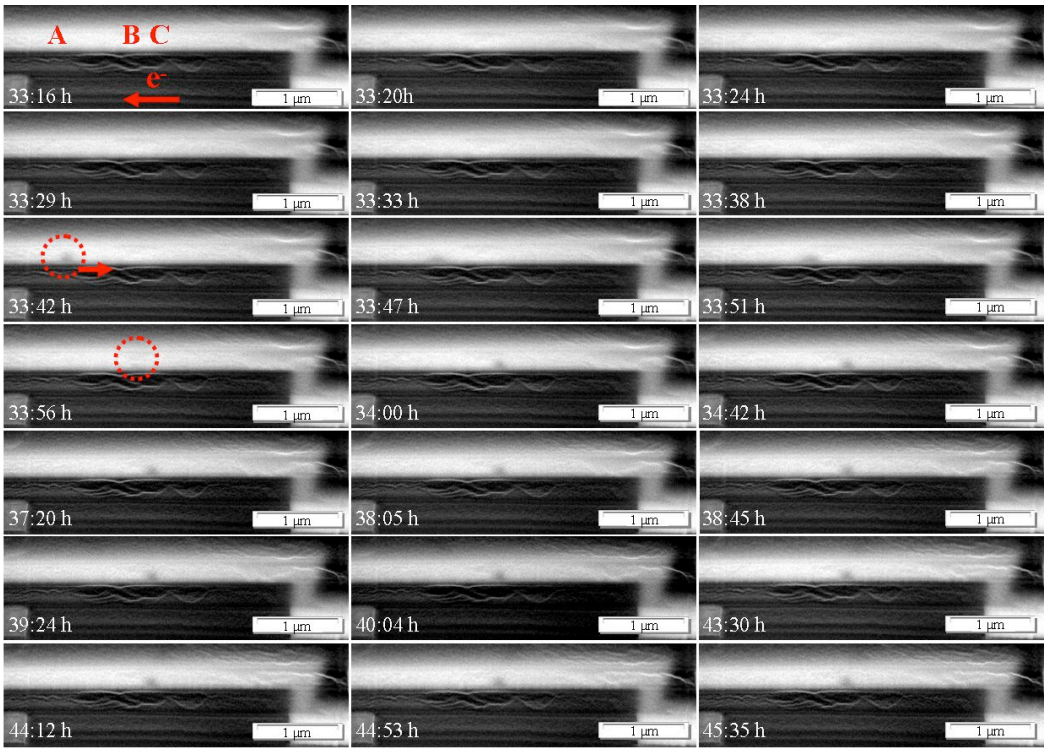
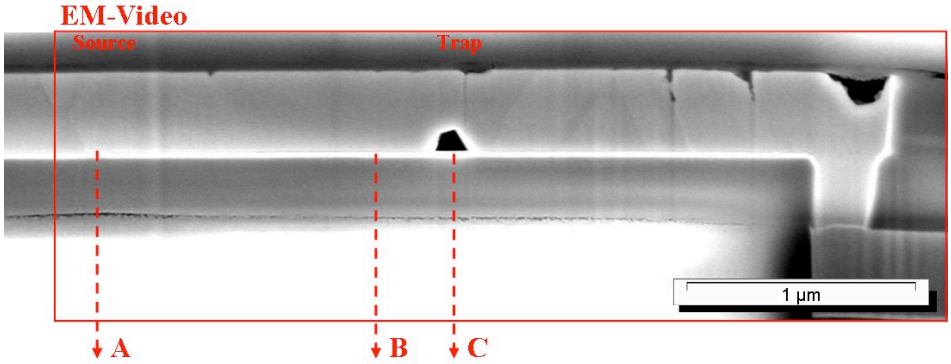
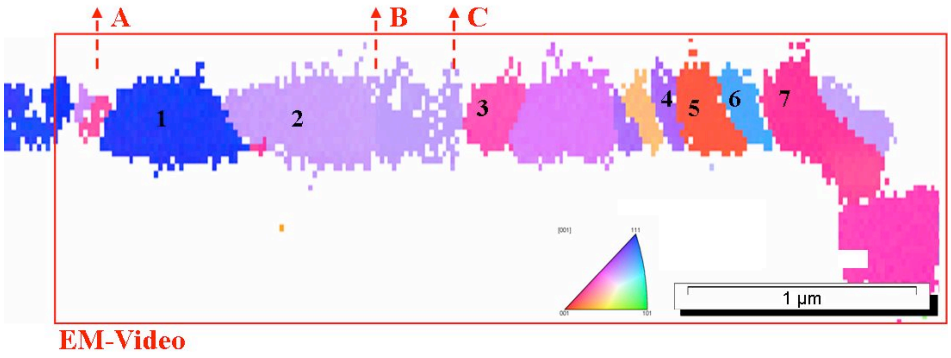


Fig. 4.15: *In-situ* SEM image sequence for CuAl-sample 4.



(a) SEM image of the cathode region.



(b) Inverse pole figure (IPF) maps.

Fig. 4.16: Post-mortem SEM/EBSD analysis of CuAl-sample 4.

4.1.4 EM in Cu/CoWP interconnects

Cu/CoWP-sample 1

Interconnect degradation vs. time Figure 4.17 shows an *in-situ* SEM image sequence of the cathode region of Cu/CoWP-sample 1. The bright spots across the surface of the sample are contaminations from the sample preparation. They did not influence the experiment. This sample is different to the other samples as in this case a Metal 1 test structure was used. This means that the current direction was downwards through the via, and then, along the lower metal line. The entire process of void formation and evolution that was observed in this sample was very inhomogeneous. All interfaces as well as the microstructure of the line were involved in the process.

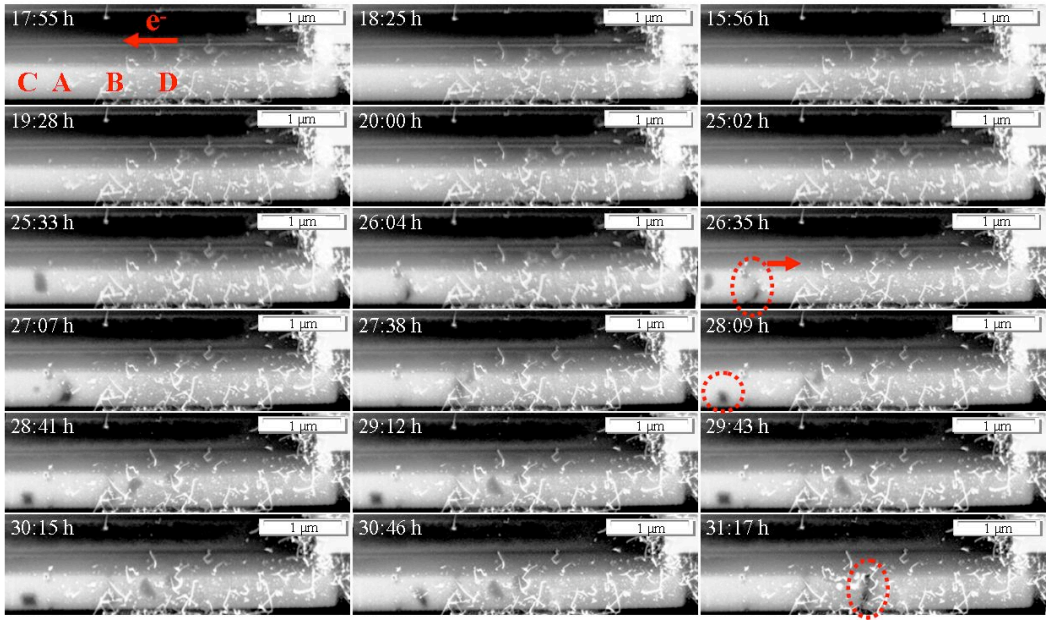
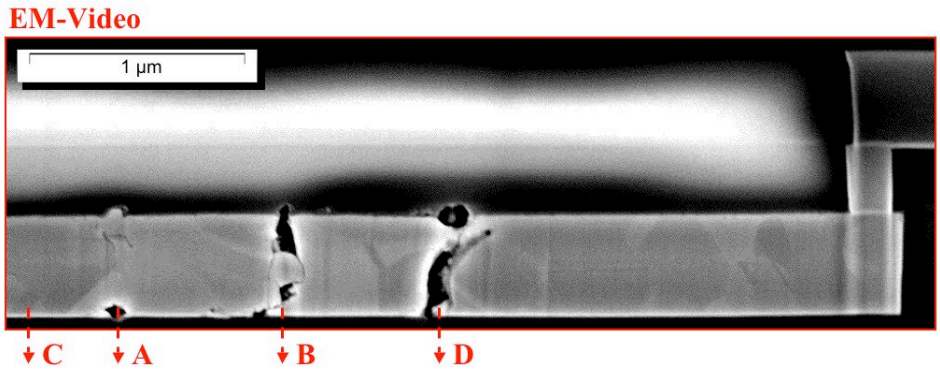


Fig. 4.17: *In-situ* SEM image sequence for Cu/CoWP-sample 1.

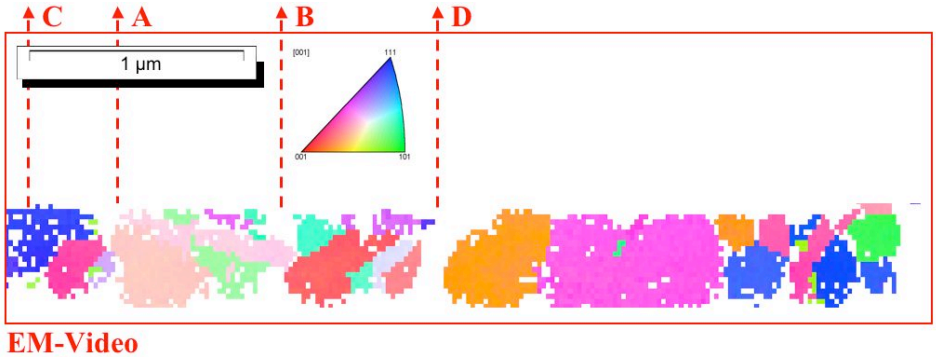
The first void appeared after 24 minutes, moving into the field-of-view from the left. It initially moved along the sidewall of the line, and it continued to move along the Cu/CoWP-coating interface for a short period of time. At position A (3.6 μm away from the line end), suddenly a slit-like void was formed that spanned across the entire line height from top to bottom. This entire process took only 6 minutes. Subsequently, the void remained at position A for a short period of time (9 minutes) while a new void appeared, moving along the same path. This second void merged into the first one, suggesting

a pathway around a certain grain along the backside of the line instead of decomposing it on the way. The newly formed, larger void maintained the slit-like shape, and it started to move towards position B (2.9 μm away from the line end) immediately. It reached position B 5 minutes later, where it remained stationary once again. It also became less visible, which indicates that it moved towards the backside of the line. 4 minutes later, a new void moved into the field-of-view. This void traveled along the Cu/barrier interface at the bottom of the Cu line up to position C (4 μm away from the line end), where it stopped. It grew slightly and developed a faceted shape. This shape is supposed to be caused by differently oriented lattice planes of the surrounding grains. In the meantime, a part of the void at position B detached from it, and moved slightly further along the line. After 16 minutes, the void at position C continued to move along the line very rapidly. It changed its shape repeatedly on its way. Finally, all voids merged together forming a slit void at position D (2.1 μm away from the line end). Due to this void the sample failed after 75 minutes. There was no voiding observed beyond position D.

Interconnect degradation vs. microstructure The IPF map in figure 4.18 shows that the slit voids that were observed at three positions during the *in-situ* SEM experiment coincide with vertical grain boundaries that span across the entire height of the line. On the cathode side of the grain boundaries reside either large grains (A and D) or a twinned region (B, depicted as a cyan-red-cyan combination of three grains). In region C, where a faceted void was observed to remain stationary for some time, a Cu<111>-oriented grain is visible above the void position as well as a Cu<511>-oriented grain on the cathode side of the void. As observed previously, such grain orientations seem to play a special role for the void movement along an interface.



(a) SEM image of the cathode region.



(b) Inverse pole figure (IPF) maps.

Fig. 4.18: Post-mortem SEM/EBSD analysis of Cu/CoWP-sample 1.

Cu/CoWP-sample 2

Interconnect degradation vs. time Figure 4.19 shows an *in-situ* SEM image sequence of the cathode region of Cu/CoWP-sample 2. This sample was tested at a lower current density than Cu/CoWP-sample 1. As a result the void formation and evolution occurred at a much lower rate. The first void was observed after 6:10 hours. It moved very slowly within 6 hours towards position A, which is 3.3 μm away from the line end. Then, it suddenly jumped towards position B (3.1 μm away from the line end) within 6 minutes. There, it remained completely stationary for the rest of the experiment. No further voids were observed. The experiment was stopped after 13:40 hours.

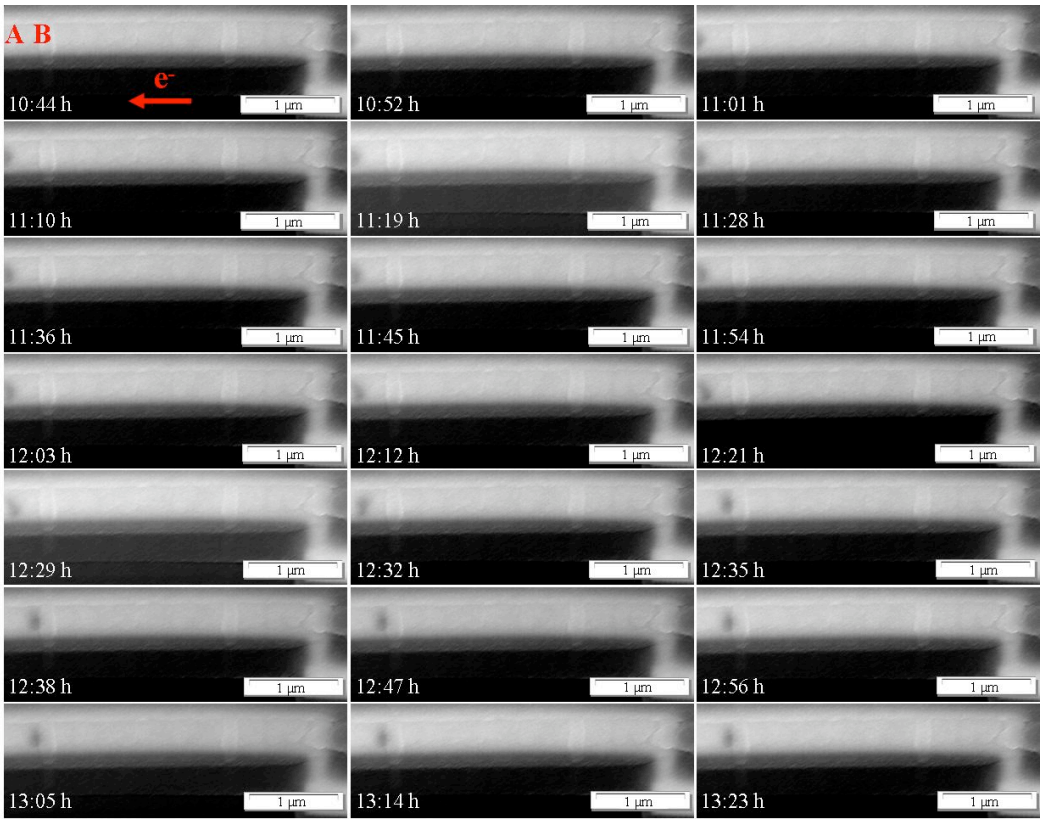
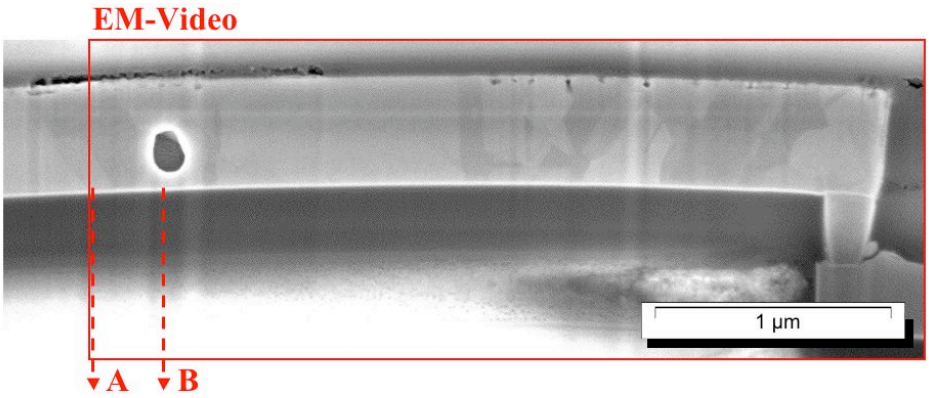
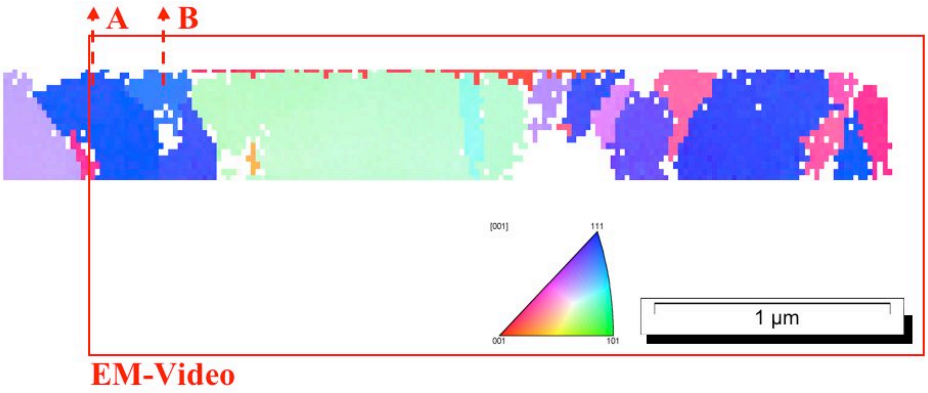


Fig. 4.19: *In-situ* SEM image sequence for Cu/CoWP-sample 2.

Interconnect degradation vs. microstructure The EBSD investigation showed that the void resides between at least three Cu<111>-oriented grains in the interior of the line (figure 4.20). It cannot be concluded from this experiment whether there was a grain of a different orientation located at that position before the void developed. The sudden jump of the void between positions A and B observed in the EM video corresponds to a <111>-oriented grain of that size.



(a) SEM image of the cathode region.



(b) Inverse pole figure (IPF) maps.

Fig. 4.20: Post-mortem SEM/EBSD analysis of Cu/CoWP-sample 2.

4.1.5 Time-to-failure distributions

Figure 4.21 shows a probability plot of the time-to-failure (TTF) distributions for Cu and CuAl interconnects, that were obtained from the *in-situ* EM experiments. The data indicate a significant improvement of the resistance against EM for the CuAl interconnects compared to the Cu interconnects. The improvement of the time-to-failure of the CuAl interconnects amounts to at least one order of magnitude.

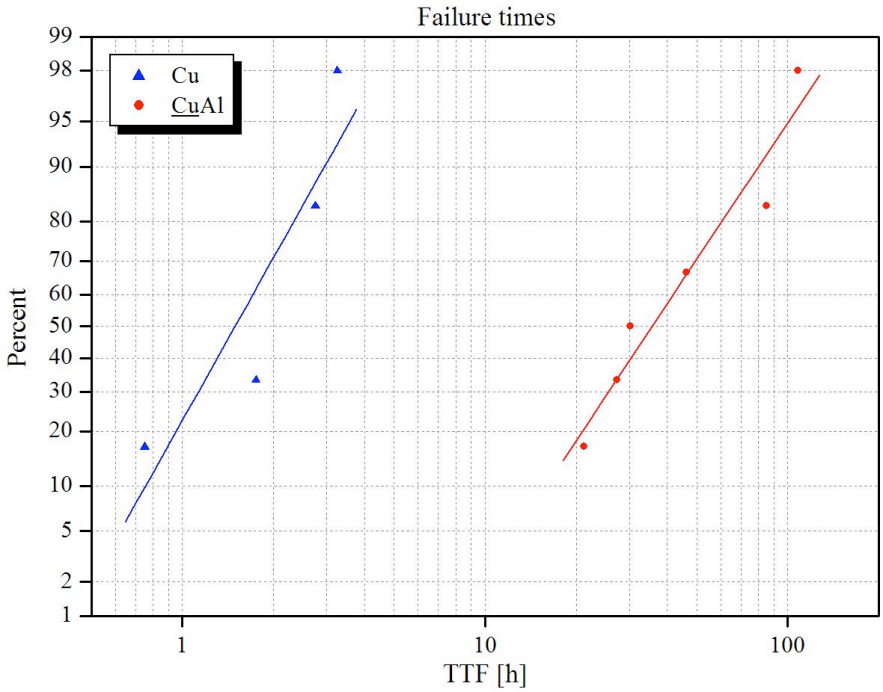
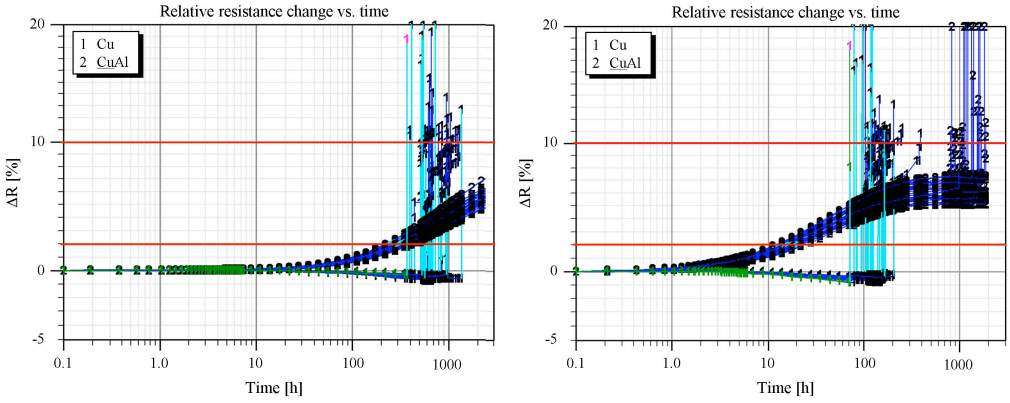


Fig. 4.21: Propability plot of EM time-to-failure for Cu and CuAl interconnects.

4.2 Standard accelerated lifetime tests

In addition to the *in-situ* SEM investigations, standard accelerated lifetime tests were performed on Cu and CuAl interconnect samples in order to determine the activation energy for EM-induced material transport. Sets of samples were stressed at two different temperatures (300 °C and 350 °C) and at a current density of 1.5 MA/cm^2. Figure 4.22 shows the resistance traces for the individual samples for both test temperatures. The Cu interconnects showed a normal EM behavior with abrupt failures after certain test times. The CuAl interconnects showed a different behavior. The resistance of the test structures started to increase continuously from the beginning of the test. At 350 °C, the resistance increase saturated and the samples eventually failed due to abrupt resistance increases. At 300 °C, the resistance increase was observed as well. However, the experiment was stopped after 3000 hours, before the resistance increase reached a plateau. No failures due to an abrupt resistance increase were recorded for the CuAl interconnects at 300 °C.



(a) Test temperature: 300 °C.

(b) Test temperature: 350 °C.

Fig. 4.22: Resistance traces from standard accelerated lifetime tests for Cu and CuAl interconnects (2 and 10 % failure criteria marked as red lines).

From these data, activation energies for the dominating material transport mechanisms were calculated for failure criteria of 2 % and 10 % resistance increase. For Cu interconnects, E_a is 1.05 eV, independent of the failure criterion. This value is higher than the expected value for Cu/SiN$_x$ capping layer diffusion (see table 2.1). Nevertheless, the *in-situ* investigations showed that the Cu/SiN$_x$ capping layer interface is the dominating material transport path. For CuAl interconnects, E_a varied significantly depending on the failure

criterion. At 2 % resistance increase, no EM failures have occured. An E_a of 1.79 eV was calculated. It is assumed, that the resistance increase is caused by Al diffusion from the TaAl barrier layer into the Cu lines. Then, the E_a value represents an activation energy for thermally activated Al diffusion from the TaAl barrier layer into the Cu lines.

A failure criterion of 10 % was used to estimate E_a for EM-induced Cu diffusion. Since there were no failures recorded in CuAl interconnects at 300 °C, two assumptions were made. The first failure was assumed to occur after 3000 hours. Furthermore, the standard deviation (σ) of the lognormal failure distribution from the 350 °C test was used. With these values, a failure distribution for 300 °C was constructed and an E_a of 1.00 eV was calculated. This value represents a lower limit. The true value should be significantly higher.

Table 4.3 summarizes the MTTF and σ values obtained from the lognormal failure distributions. The activation energies for material diffusion are given in table 4.4.

Table 4.3: Results of the accelerated lifetime tests.

Interconnect type	**MTTF**$_{300}$ **[h]**	σ_{300}	**MTTF**$_{350}$ **[h]**	σ_{350}
Cu	697	0.34	131	0.35
CuAl	n.a.	n.a.	1495	0.37

Table 4.4: Activation energies for material diffusion in Cu and CuAl interconnects.

Interconnect type	E_a**(2 %) [eV]**	E_a**(10 %) [eV]**
Cu	1.05	1.03
CuAl	1.79	1.00

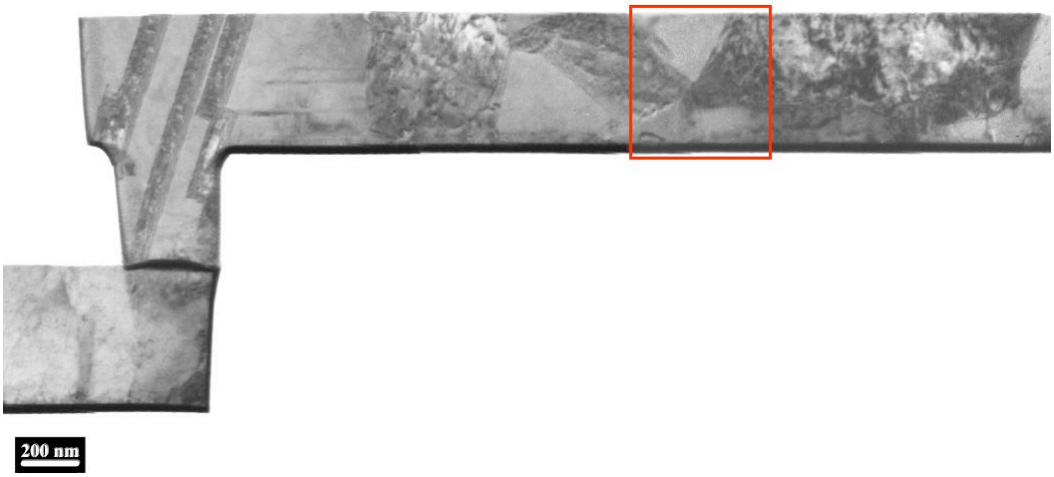
4.3 Analysis of unstressed reference samples

4.3.1 Spatial distribution of Al in CuAl interconnects

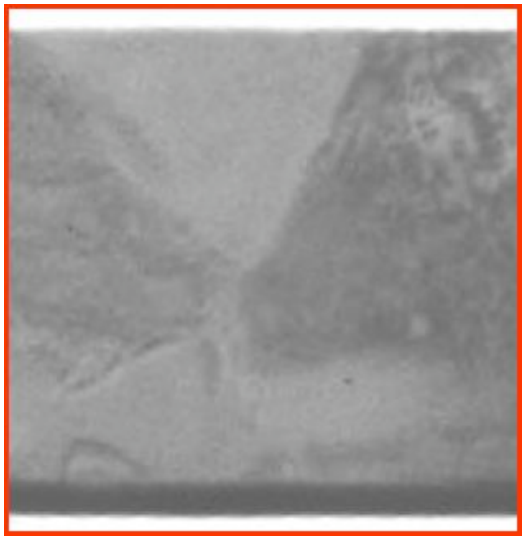
The spatial distribution of Al within fully processed CuAl interconnects was studied using TEM/EDS. It was found in all maps that Al is predominantly located at the Cu grain boundaries. Additionally, a significant enrichment of Al was found to be present at the top interface of the metal line between Cu and the SiN_x capping layer.

Figure 4.23 shows an overview image (a) and a magnified image of the EDS mapping area (b), together with the corresponding Al map (c). Several grain boundaries can be seen in image (b). The Al map (c) shows an enrichment of Al at the grain boundaries as well as at the Cu/capping layer interface. The width of the Al enrichment at the grain boundary in the center of image (c) seems to be relatively large. This observation can be an artifact, attributed to the fact that the grain boundary is not aligned perfectly normal to the sidewall of the TEM sample.

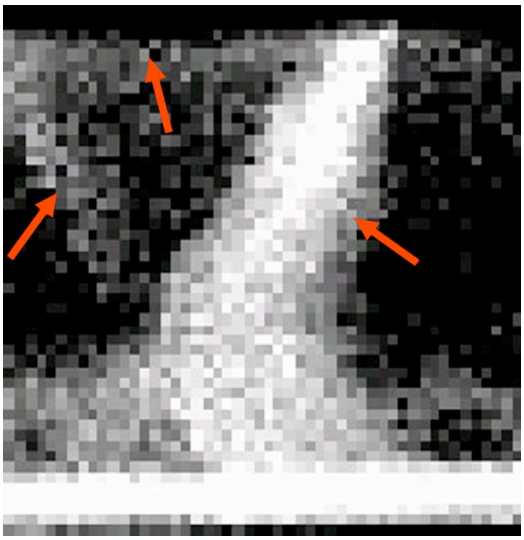
In all acquired Al maps, the highest Al concentration was always detected at grain boundaries. Quantitative spot analyses at grain boundaries showed that the Al concentration ranged from about 2 to 4 at.-% Al in Cu. On one occasion a concentration as high as 10 at.-% Al in Cu was measured. The concentration of Al at the Cu/capping layer interface was detected to range from about 1 to 3 at.-%. The concentration of Al within the Ta barrier layer could not be determined because of the high background of the spectrum near the Al peak at 1.487 keV.



(a) TEM brightfield image: overview, EDS mapping area (red square).



(b) TEM brightfield image: EDS mapping area.



(c) Al map: enrichment at grain boundaries and top interface (red arrows).

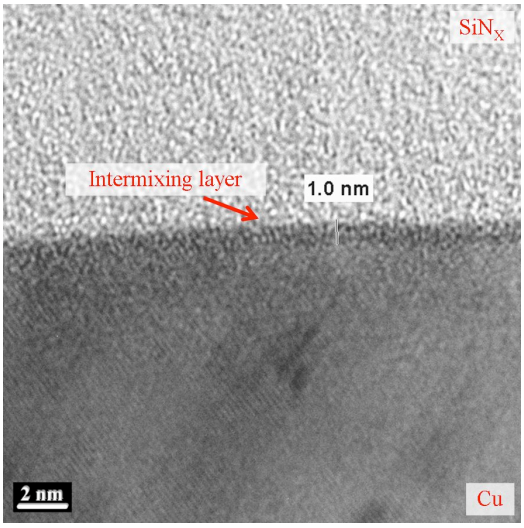
Fig. 4.23: Spatial distribution of Al in CuAl interconnects.

4.3.2 Atomic structure of the Cu/capping layer interface

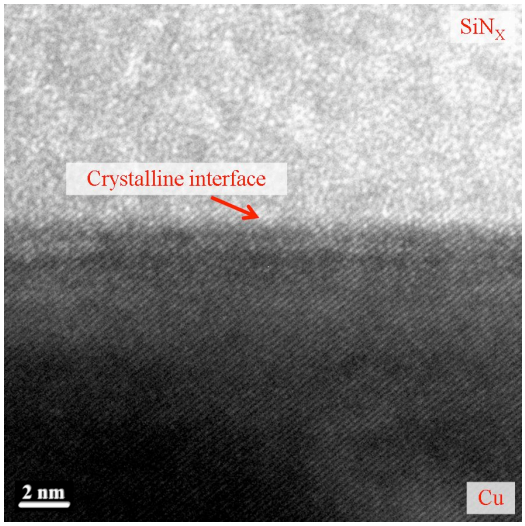
The HR-TEM investigations of the Cu/capping layer interfaces of Cu and CuAl interconnects as well as Cu/CoWP interconnects revealed distinct differences. Figure 4.24 provides an overview image as well as individual HR-TEM images for the three types of interconnects. The overview image (a) shows the cathode via region of the EM test structure.

The Cu/capping layer interface of the pure Cu interconnect sample (b) is characterized by an amorphous "intermixing layer" of about 1–2 nm thickness with a high degree of disorder. In contrast to that, lattice planes are visible at the Cu/capping layer interface of the CuAl-interconnect sample (c) that extent up to the top interface. There is no "intermixing layer" present. The interface is highly ordered and the Cu lattice planes appear almost completely undisturbed. In the Cu/CoWP sample (d) the intermediated metallic CoWP-coating can be seen as the marbled region between the Cu and the SiN_x layer, spanning almost across the entire image. At the interface between Cu and CoWP, lattice planes can be seen in both metal films sometimes without any interruption at the interface. This kind of interface with regions of coherence (epitaxy-like growth) is highly ordered.

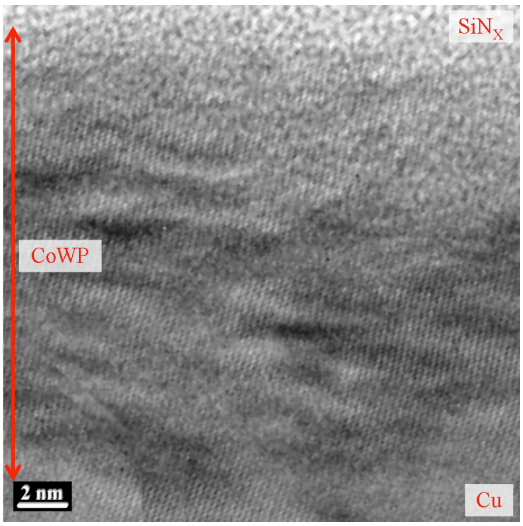
(a) Brightfield TEM image: overview.



(b) Cu interconnect: top interface.



(c) CuAl interconnect: top interface.



(d) Cu/CoWP interconnect: top interface.

Fig. 4.24: HR-TEM images of the capping layer interface of different types of Cu-based interconnects.

4.3.3 Cu microstructure

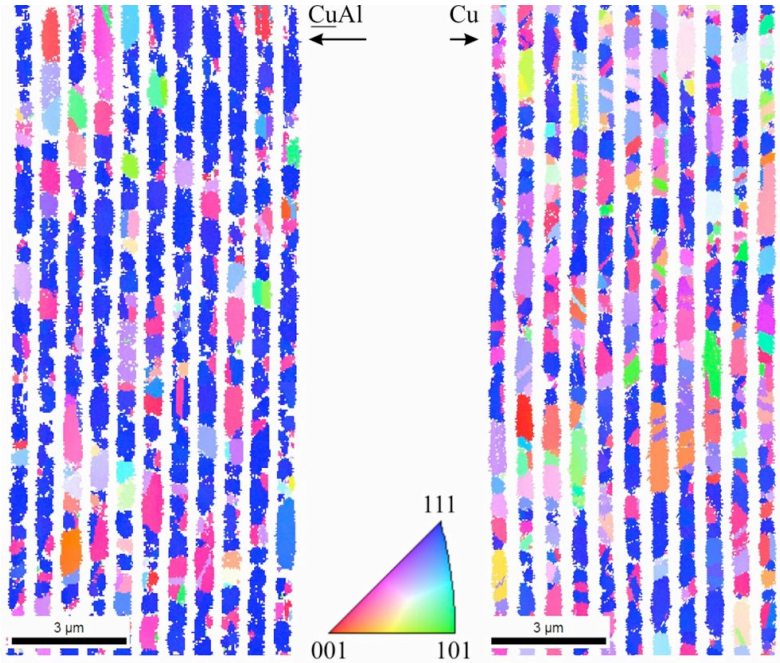
The microstructure of unstressed reference samples was investigated applying SEM/EBSD. In this study, 17 μm long segments of the EM test structures were scanned with a step size of 40 nm.

Local orientation and texture

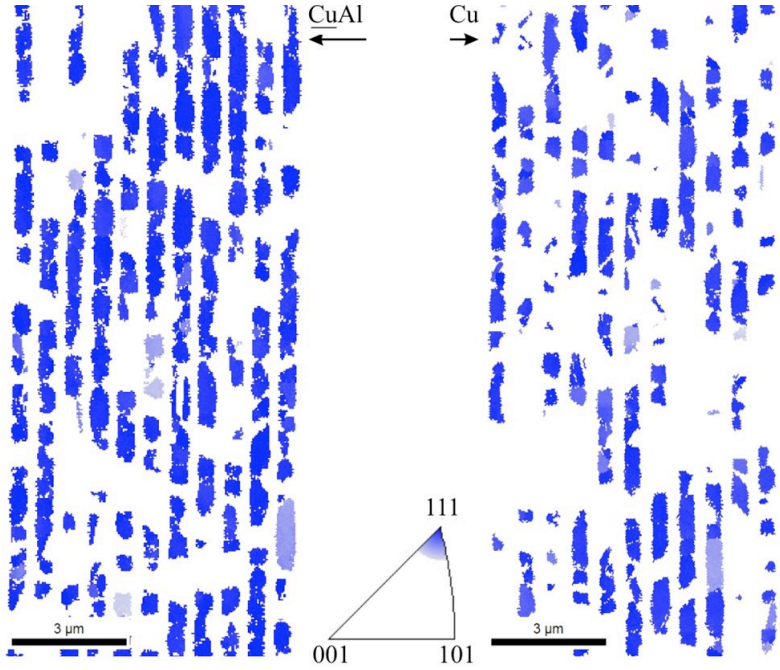
In figure 4.25(a), IPF maps are depicted for both types of interconnects. In these maps, each grain is colored according to its crystallographic orientation relative to the sample normal direction (ND). The unit triangle of the inverse pole figure provides the color key for the IPF maps. For both types of interconnects a large amount of Cu<111>-oriented grains can be seen.

The Cu<111> crystal direction maps in figure 4.25(b) further emphasize this observation. Here, only those grains are shown in blue where the Cu<111> crystal direction is within a 10 ° tolerance angle to the sample normal. It is evident that the CuAl sample shows a larger fraction of Cu<111>-oriented grains. In order to quantify this apparent texture difference between the two types of interconnects further, two parameters were extracted from the EBSD data, the surface area fraction of Cu<111>-oriented grains and the intensity of the center peak of Cu(111) pole figures.

Figure 4.26 provides the Cu(111) pole figures as well as the results of the quantitative texture analysis. The pole figure of the CuAl sample appears much sharper compared to the pole figure of the Cu sample. Both quantitative parameters, the surface area fraction of Cu<111>-oriented grains as well as the center peak intensity of the Cu(111) pole figure, show that the CuAl interconnects are significantly stronger <111>-textured. About 63 % of the surface area of the CuAl-interconnects show a Cu<111> crystal orientation, compared to only 40 % for the Cu interconnects. The center peak intensities of the Cu(111) pole figures are 33 and 21, respectively.

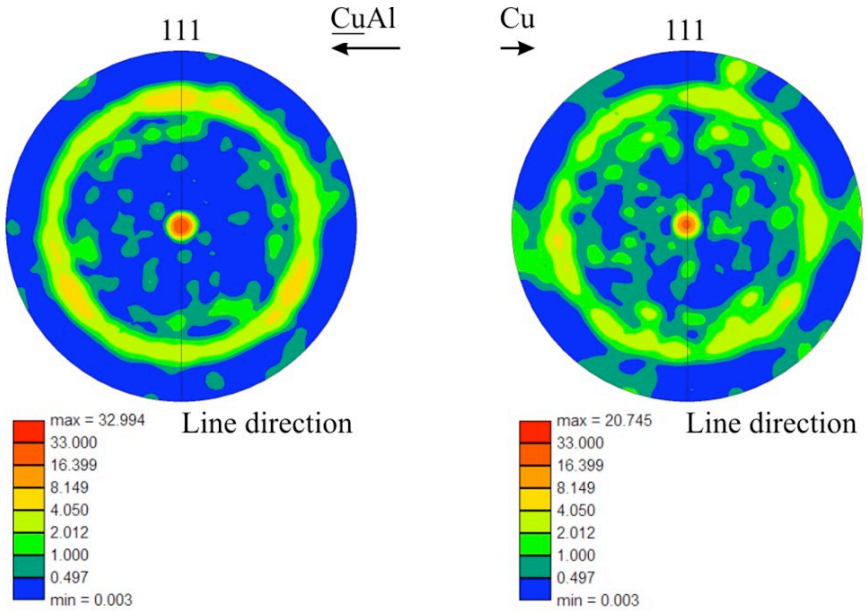


(a) IPF maps.

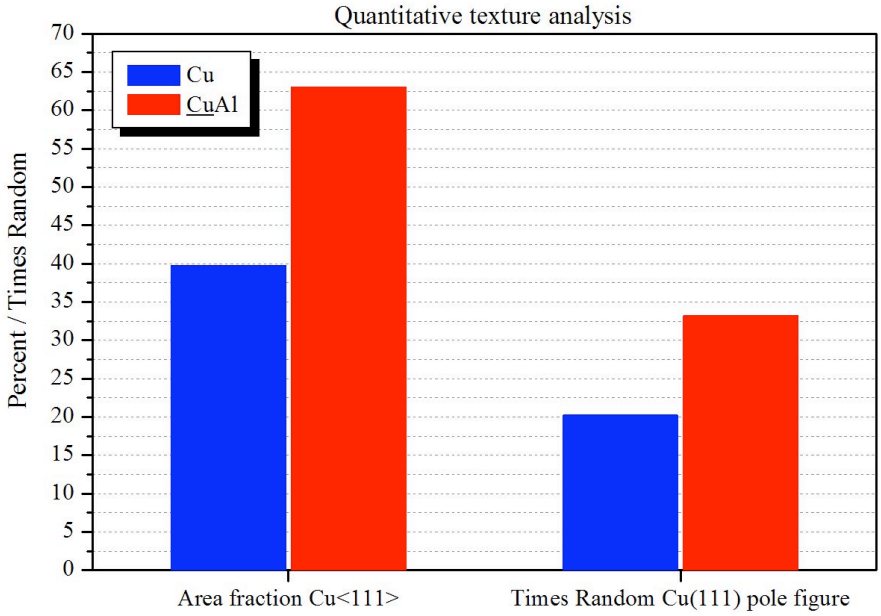


(b) Cu<111> crystal direction maps (tolerance angle: 10 °).

Fig. 4.25: Inverse pole figure (IPF) maps and Cu<111> crystal direction maps of CuAl and Cu interconnects.



(a) Cu(111) pole figures.



(b) Quantitative texture analysis.

Fig. 4.26: Cu(111) pole figures and quantitative texture analysis of CuAl and Cu interconnects.

Grain size distribution and twin boundary characterization

From the EBSD investigations quantitative information about the grain size distributions as well as the grain boundary properties of the samples were obtained. Figure 4.27 shows unique grain color maps for both types of interconnects, CuAl and Cu. The black lines in these maps highlight Σ-3 or twin boundaries.

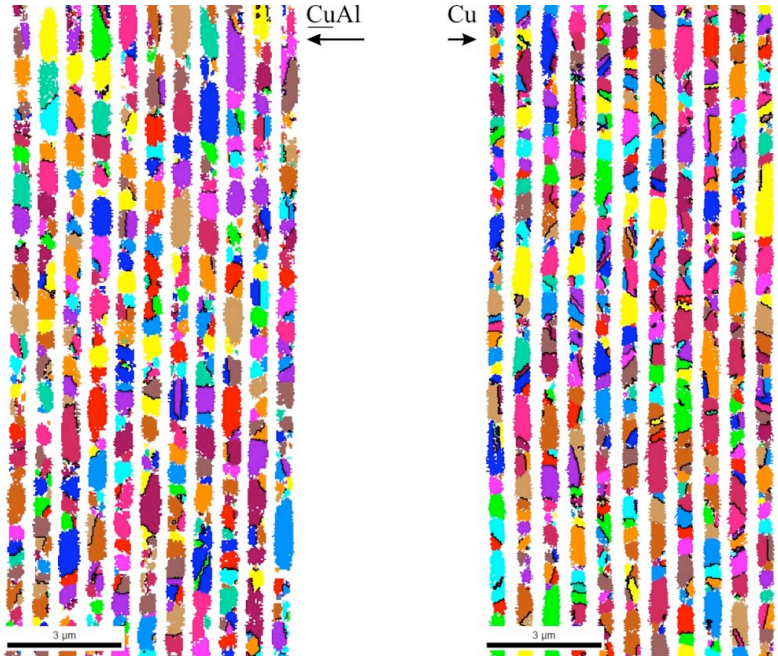


Fig. 4.27: Unique grain color maps for CuAl and Cu interconnects. Twin boundaries (Σ-3) were drawn as black lines.

The general appearance of both maps suggests that the grain growth is controlled by the linewidth as most grains span across the entire line. However, there are numerous small grains visible between larger grains as well as at the line edges. The Cu interconnects appear more finely grained than the CuAl interconnects with more Σ-3 boundaries present. Figure 4.28 shows a probability plot of the grain size distributions of the two types of interconnects. The distribution of the CuAl sample is wider than that of the Cu sample, with a tendency towards large grains. The amount of small grains below 150 nm is very high in both samples. This result can be partly explained by the spatial resolution of the scans with a fixed step size of 40 nm, i.e. narrow grains are divided into multiple small grains. Due to this effect, the error of the grain detection algorithm is relatively large for small grain

sizes. On the other hand, there are many clusters of real small grains present between larger ones. This prohibits the use of more aggressive filter parameters. Consequently, the statistical mean grain diameter obtained from EBSD measurements tends to be smaller than that obtained by other techniques, such as the line-intercept method [21].

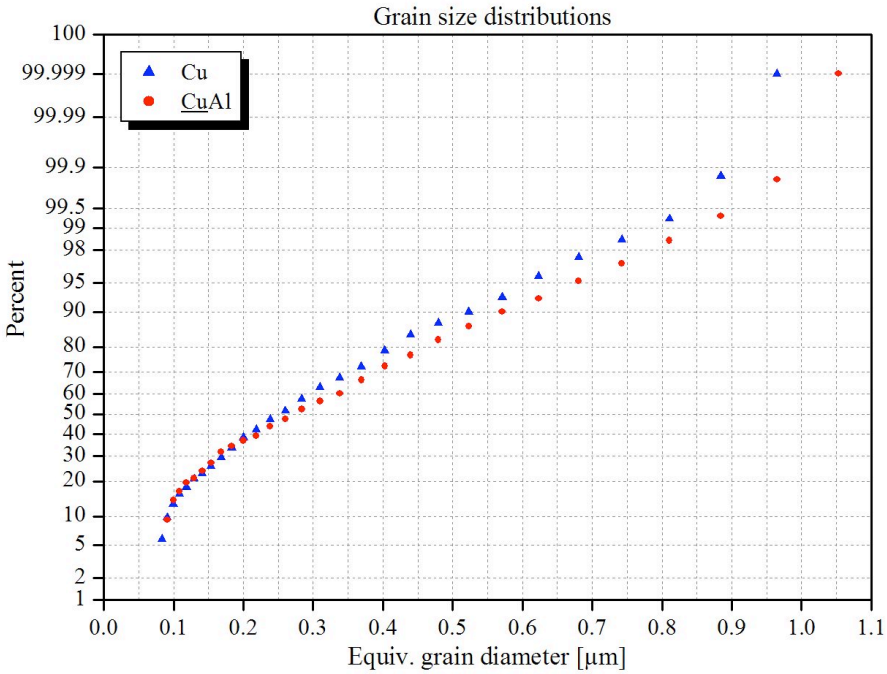


Fig. 4.28: Probability plot of grain size distributions of CuAl and Cu interconnects.

Table 4.5 summarizes the quantitative analysis of the microstructure of the investigated CuAl and Cu interconnects. The difference of the mean values for the grain diameters is smaller than expected from the orientation maps. This is due to the large fraction of small grains in both samples. The minimal grain diameter of 90 nm represents an artificial lower limit imposed by the experimental settings during the EBSD data acquisition.

In order to assess the amount of grain twinning, three parameters were extracted from the EBSD raw data, the length of Σ-3 boundaries, the total length of grain boundaries and the ratio and difference of the two. The total length of grain boundaries is considerably larger for the Cu interconnects compared to the CuAl interconnects. The length of non-Σ-3 boundaries is almost identical in both samples. However, the fraction of Σ-3 boundaries is significantly larger for the Cu interconnects as well. This observation confirms

that the Cu interconnects exhibit generally smaller grains and more recrystallization twins. That means, the larger grain size in CuAl interconnects has to be attributed to the lack of twins.

Table 4.5: Grain sizes and twin fractions.

Parameter	**Cu**	**CuAl**
Mean grain diameter [nm]	309	321
Max. grain diameter [nm]	980	1020
Total GB length [μm]	271	201
Σ-3 GB length [μm]	161	98
Non-Σ-3 GB length [μm]	110	103
Σ-3 GB fraction [%]	60	49

4.3.4 Electrical resistance and temperature coefficient of resistivity

In this study, resistance measurements on via and line test structures were performed on two occasions during wafer processing. Initially, they were measured directly after Metal 5-polish. A second measurement was taken after the wafers had been fully processed. This means that the wafers were subjected to the thermal treatments associated with the processing of three additional levels of metallization. The measurements were performed on lots of 12 wafers for each interconnect type.

Figure 4.29 shows sheet resistance data for the Metal 5 test structure as well as resistance data for the Via 4 test structure. The sheet resistance is a measure of resistivity of thin films with a uniform thickness. It is commonly used in semiconductor industry to describe the resistivity of two-dimensional systems, such as interconnect lines or doped semiconductor regions. It derives from the expression for the resistance of a regular conductor:

$$R = \rho \frac{L}{A} = \frac{\rho}{h} \cdot \frac{l}{w} \tag{4.2}$$

The term

$$Rs = \frac{\rho}{h} \tag{4.3}$$

is called sheet resistance. ρ is the resistivity and l is the length of the conductor. A is the cross-sectional area. It can be split into the width w and

the sheet thickness or height h. From equation 4.2 follows that the unit for Rs is Ohm. However, to avoid confusion between R and Rs, the unit of Rs is specified as "ohms per square". The l/w ratio can be thought of as the number of unit squares (of any size) of material in the resistor.

The CuAl interconnects exhibited a 35 % increase in Metal 5-Rs after full processing compared to Metal 5-polish. Also, the width of the Rs distribution is slightly increased. Directly after Metal 5-polish, Rs was identical to that of the Cu interconnects. The Cu interconnects showed no significant increase in Metal 5-Rs after full processing. The Via 4 resistance of the CuAl samples was found to be 13 % higher than that of the Cu samples. There was no significant resistance increase observed between the two measurements for the via test structures.

From the Rs measurements, the resistivity of the interconnect materials was determined by correcting for the cross-section areas according to the equations described above. The increase in resistivity for the CuAl samples amounted to about 42 %. Table 4.6 summarizes the electrical properties of the samples after full processing.

Table 4.6: Sheet resistance and resistivity of Cu and CuAl interconnects.

Type	**M5-Rs [Ω/square]**	**M5-ρ [$\mu\Omega$cm]**	**Via4-R [Ω]**
Cu	0.058	2.20	0.520
CuAl	0.078	3.12	0.584

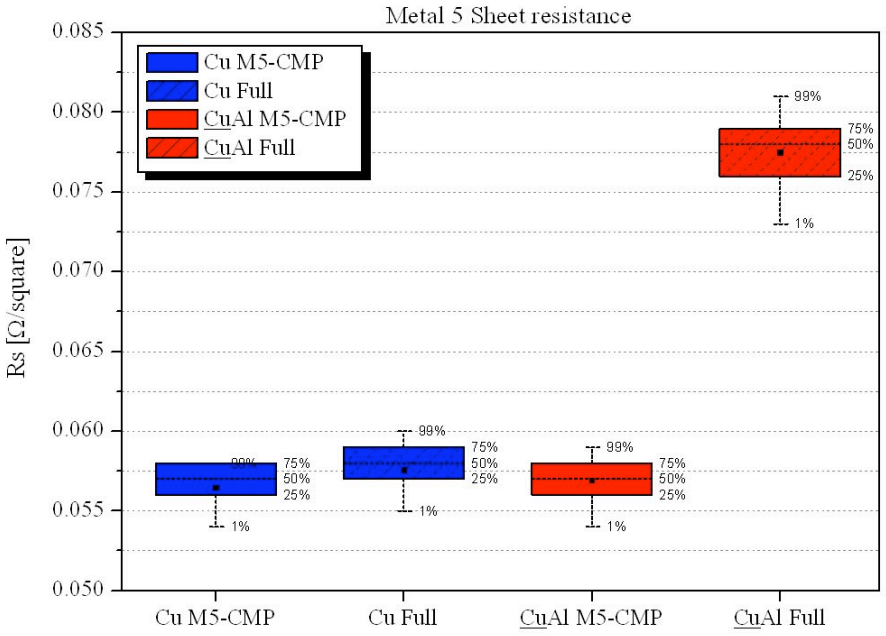
In addition to the wafer-level resistance measurements, the temperature-dependence of the resistance of the EM test structures was measured and the temperature coefficient of resistivity (TCR) was determined using the following equations.

$$R = R_0(1 + TCR(T - T_0)) \tag{4.4}$$

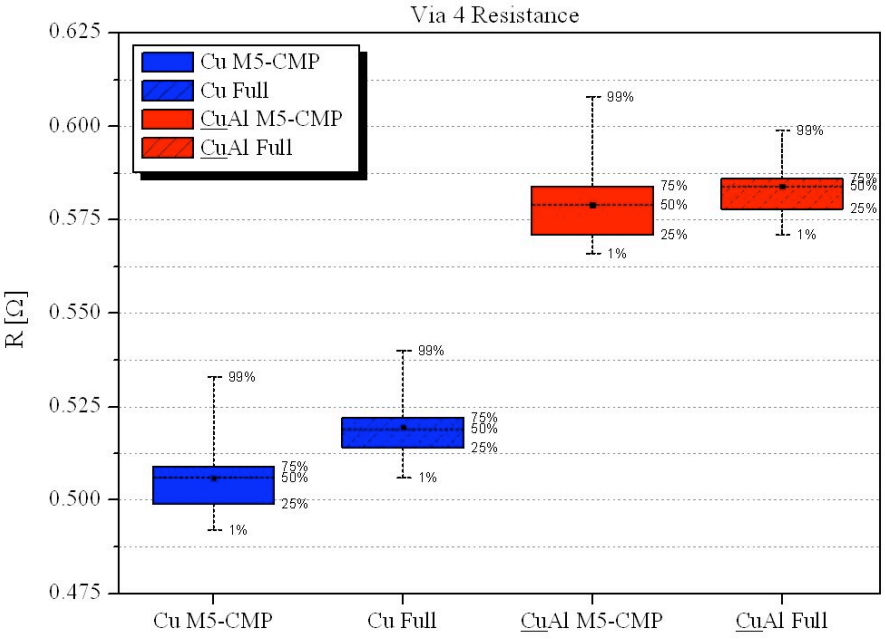
where R is the resistance at the temperature T and R_0 the resistance at the reference temperature T_0. Rearranging equation 4.4 yields

$$TCR = \frac{S}{R_0} \tag{4.5}$$

where S is the slope of the linear fit curve and R_0 the resistance at $T_0 = 0\,^{\circ}\mathrm{C}$, which can be found as the intersection with the R-axis.



(a) Metal 5 sheet resistance of CuAl and Cu interconnects.



(b) Via 4 resistance of CuAl and Cu interconnects.

Fig. 4.29: Metal 5 sheet resistance and Via 4 resistance of CuAl and Cu interconnects.

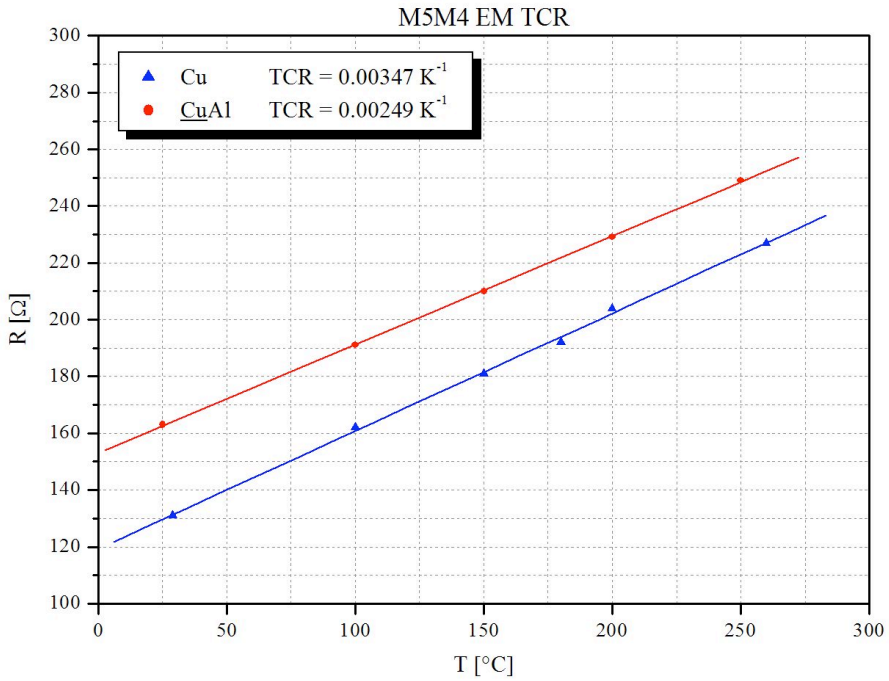


Fig. 4.30: Temperature-resistance curves of CuAl and Cu interconnects.

Figure 4.30 shows the temperature-resistance curves measured on EM test structures. The calculated values for TCR are also given. The resistance of the EM test structures of the CuAl samples was 26 % higher than that of Cu samples at room temperature. The TCR of the CuAl interconnects was 39 % lower than that of the Cu interconnects. These measurements were used to calibrate the experiment temperatures during the *in-situ* SEM experiments.

Chapter 5

Summary and discussion

5.1 Summary of EM experiments

The experiments revealed a significant improvement of at least one order of magnitude in the time-to-failure for CuAl and Cu/CoWP interconnect samples compared to Cu interconnects. In some cases, the experiments on CuAl or Cu/CoWP samples had to be aborted before the samples failed. Furthermore, the *in-situ* SEM experiments visualized fundamentally changed degradation mechanisms in CuAl and Cu/CoWP interconnects compared to pure Cu interconnects.

5.1.1 Cu interconnects

In standard Cu interconnects, the Cu/SiN_x capping layer interface was found to act as the fast diffusion path as shown in most of the other studies. However, the void nucleation did not occur solely at the via site, as often assumed in literature. Instead, voids were mostly formed away from the via at the Cu/capping layer interface. Failures occurred after the voids migrated towards the cathode end of the line above the via, where they agglomerated and eventually grew down into the via. The virtual movement of voids along the Cu/SiN_x capping layer interface was discontinuous process. Voids often stopped for extended periods of time before continuing to move. In some cases, voids were trapped entirely at certain positions. Post-mortem analyses showed that the Cu/SiN_x capping layer interface was usually restored completely after a void had passed along it. Typically, no signs of remaining voids

or delaminations were observed at that interface if the experimental conditions were not chosen too aggressively. Often a substantial redeposition of material into the upper part of the vias was observed during the final stage of an experiment.

5.1.2 CuAl interconnects

The degradation mechanisms that were observed on this type of samples were significantly different compared to pure Cu interconnects. Only a few samples showed void nucleation and evolution along the Cu/SiN_x capping layer interface. Moreover, these voids were not important for the failure of the samples. Instead, the main location for void nucleation was the Cu/barrier interface at the bottom of the Cu lines, several micrometers away from the cathode via. Voids were usually formed there, and then they migrated towards the via. Similar to pure Cu interconnects, the void evolution was very discontinuous. Voids moved relatively slowly and were often trapped entirely at some distance away from the via. Other voids moved much faster along the Cu/barrier interface into the via. This effect was often observed in the later stages of the experiments after several tens of hours. The via voids usually caused the failure of the samples. TEM/EDS analyses on stressed samples revealed that the inner Cu surface of trapped voids was covered with Al. Furthermore, it was found that the initially increased Al concentration at grain boundaries was not evident on stressed samples anymore. The Al enrichment at the Cu/capping layer interface was still there.

The results of the standard accelerated lifetime tests showed that a continuous diffusion of Al from the TaAl layer into the Cu lines occurred during long thermal treatments. It was concluded from these observations, that the Al distribution within the Cu grains became more uniform during long EM experiments. It is important to note, that the diffusion barrier functionality of the TaAl layer was not degraded.

On a minority of CuAl samples, a second failure mechanism was observed. In this case, the voids nucleated at the Cu/capping layer interface at some distance away from the via. No movement of the voids was observed. Instead, they grew to considerable sizes, while the removed material piled up into hillocks directly adjacent to the voids on their anode side. Such samples failed either due to extrusion shorts or due to large voids in the line away from the via. It is important to note, that this failure mechanism was only observed during a retest of some sample two years after the wafers were processed. The reason for this effect is not understood so far.

5.1.3 Cu/CoWP interconnects

CoWP-coated Cu interconnects proved to be very resistant against EM. A void formation could only be observed under extreme stressing conditions, i.e. very high temperatures combined with high current densities. Then, voids were formed far away from the via. Especially the Cu/barrier interfaces as well as the microstructure of the Cu lines were involved in the process. The samples usually failed due to slit-like line voids that were eventually formed at some distance away from the via. The positions of these voids coincided with vertical grain boundaries. The interface between Cu and the CoWP-coating appeared crystalline and highly ordered. Lattice planes extended across the interface from Cu into CoWP.

5.2 Discussion

5.2.1 Effect of interface strength

The significantly improved lifetime of CuAl and CoWP-coated Cu interconnects is connected with a fundamental change of the degradation mechanism. The difference can be explained based on the atomic structure of the Cu/capping layer interface of the three types of interconnects. Two distinct differences were found. The characteristic intermixing layer at the Cu/SiN_x capping layer interface of pure Cu interconnects is missing in CuAl and Cu/CoWP samples. Instead, the interfaces between Cu and the capping layers (SiN_x or CoWP) were crystalline for these samples. Furthermore, considerable amounts of metal atoms were present at the Cu/capping layer interfaces, either as component of an alloy (CuAl) or in the form of an additional layer (CoWP).

In the case of CuAl interconnects, there exist two factors that contribute to the increased strength of the Cu/capping layer interface: the presence of Al atoms and the crystalline structure of the interface. Based on the Al concentration that was measured at the Cu/capping layer interface, a continuous Al coverage along the entire interface is unlikely. On the other hand, recent investigations suggest that a crystalline interface alone cannot account for the significant gains in EM lifetime observed in these samples. Instead, the chemical nature of impurities has to be the dominating factor. This conclusion is supported by observations from other studies: Unintentional oxidation of the Cu surface prior to the deposition of dielectric capping layers is known to result in reduced

lifetimes. Silicidation of the Cu surface has yielded in moderate improvements but seems to be sensitive to process variations even if the interface remains crystalline [26]. Significant improvements in lifetime of at least one order of magnitude or more were only reported for samples with metallic impurities of some kind incorporated at the Cu/capping layer interface. These metal atoms form dominant metallic bonds with the Cu atoms. This effect results in an increased strength of the Cu/capping layer interface [23, 42, 52].

During the discussion of the EM reliability of Cu interconnects, the interfacial adhesion or bonding strength is of special interest. Lane *et al.* reported a relationship between the intrinsic work of adhesion and the time-to-failure for different capping layers and surface treatments [32]. They showed that the stronger the adhesion and the more reactive the bonds are, the slower is the diffusion along the interface. For CoWP-coated interconnects the interface debond energy was found to exceed the capabilities of the measurement apparatus. This result was explained with the metallic nature of the bonds.

There are no adhesion data available for CuAl interconnects. However, the observed failure mechanism suggests that the interfacial adhesion is greatly improved and in the range of that of CoWP-coated interconnects. This result leads to the conclusion that the nature of the chemical bonds at the Cu/capping interface is much more important than its atomic structure. If Cu atoms at the interface can form metallic bonds with atoms of a coating or an alloying element, their mobility is reduced significantly, and they become effectively pinned at their positions. The activation energy for EM-induced material transport in CuAl interconnects was found to be larger than 1.00 eV, which supports this conclusion.

5.2.2 Microstructure effects

The *in-situ* SEM investigation provided a large amount of evidence for the influence of the local microstructure on the EM-induced void formation and evolution processes. Post-mortem SEM/EBSD analyses showed that clusters of small grains in otherwise bamboo-like interconnects act predominantly as void nucleation sites. Alternatively, such clusters can also act as trapping sites for voids. Furthermore, there is evidence for the fact that Cu<111>-textured line regions serve as void nucleation sites. Also, such regions were found to exhibit a relatively high diffusivity compared to other regions. The EBSD investigations also revealed that grains with certain grain orientations showed a higher resistance against EM-induced decomposition than others. In particular, Cu<511>-oriented grains that were located on the cathode side

of Cu<111>-oriented line regions acted as blocking grains for material transport and hence stopped the movement of voids. It is important to note, that this effect was observed in all three types of interconnects and on both interfaces, the Cu/capping layer interface as well as the Cu/barrier interface. Cu<511>-oriented grains are typically considered as coherent twins of neighboring Cu<111>-oriented grains. Another finding was, that material redeposition occurred by epitaxy-like growth of grains adjacent to the voids. No new grains were formed in the redeposition process.

In CuAl interconnects, trapped voids were located at intersections of grain boundaries with the Cu/barrier interface at the bottom of the interconnect line. However, the data do not allow to conclude on certain orientation relationships between neighboring grains. Instead, it was found that the inner Cu surface of the voids was covered with Al.

Void nucleation and evolution were found to be discontinuous processes. Void nucleation occurred randomly along the lines, independent of the type of interconnect. The post-mortem investigations of several samples showed that the voids often nucleated at clusters of small grains or at intersections of grain boundaries with the interface. Lloyd *et al.* proposed a model for void nucleation based on microstructure-related variations of the normal stress component along the line [40]. The model is based on the fact that the elastic constants of Cu are highly anisotropic in nature. In an interconnect segment that is subjected to EM, a hydrostatic stress gradient develops that opposes the EM driving force (Blech effect [8]). In Lloyd's model, the normal stress component of the stress gradient is modulated based on the anisotropy of Cu depending on the crystallographic orientations of the grains along the line. The criterion for void formation is defined as a critical normal stress at the interface where a delamination would occur. The model is further developed to account for the influence of grain boundaries on the local variations of the normal stress component. It is shown that strong stress dipoles can develop where the stress changes from tensile to compressive across a grain boundary.

Some of the observations from the *in-situ* investigations can be explained based on Lloyd's model. The initial voids observed at the Cu/capping layer interface of pure Cu interconnects were generally very shallow. A delamination would also be characterized as a shallow separation between two adjacent materials. Furthermore, voids often nucleated above Cu<111>-oriented grains or above clusters of small grains. According to the model, Cu<111>-oriented grains exhibit the highest normal stress component, about 40 % higher than that of Cu<100>-oriented grains. As a result, delaminations should occur more easily above Cu<111>-oriented grains. The model also predicts grain boundary

regions as positions of extreme stress gradients. Consequently, void nucleation at such position is expected. The same considerations can be used to explain the trapping of voids. The investigations revealed that voids were trapped at grain boundaries or clusters of multiple small grains. If the combination of grain orientations across a grain boundary produces a localized stress gradient that counterbalances the EM driving force at that position, a void will be trapped there.

Sukharev *et al.* showed that such gradients are possible in real interconnects. Experimental results provided by this study were used as input data for the simulation of stress profiles along the Cu/capping layer interface of pure Cu interconnect segments [69]. Sukharev's model, similar to Lloyd's model, predicts significant variations of the local stresses along an interconnect line, depending on the microstructure. Figure 5.1 shows the simulated profile of the shear stress along the Cu/capping layer interface of Cu-sample 2 (see section 4.1.2). The simulation was based on the real microstructure of this sample. Two pronounced peaks with strong gradients can be seen in the stress profile (positions B and C). During the *in-situ* SEM experiment, position B was identified as a void nucleation site, while position C acted as a trapping site. This opposite behavior can be explained with the opposite signs of the shear stress at these positions. The simulation results are in good agreement with the experimental observations.

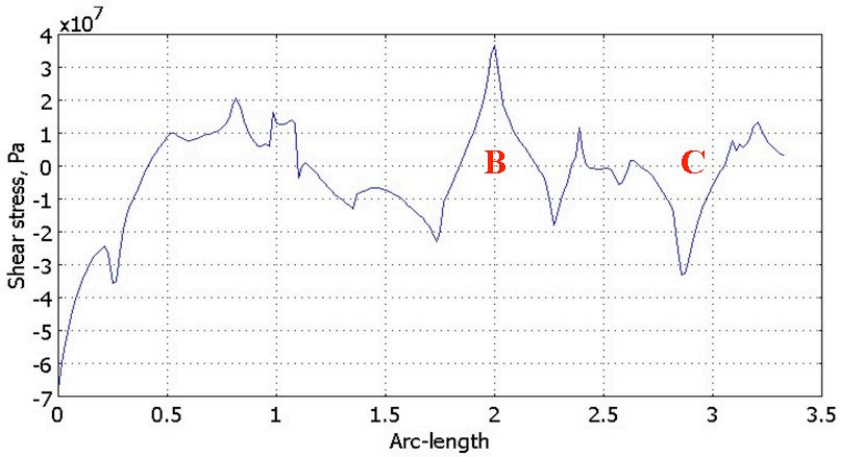


Fig. 5.1: Simulated shear stress profile along the Cu/capping layer interface of Cu-sample 2 [69].

Void nucleation in CuAl interconnects can be explained in a similar way. However, according to the models, the Cu/barrier interface would be the weaker one in terms of adhesion, since the voids were observed there. This result is somewhat surprising since it is a pure metal-to-metal interface, whereas the Cu/SiN_x capping layer interface contains significant amounts of Si and N. A possible explanation could be that some non-metal contaminations were introduced between the TaAl barrier and Cu seed deposition steps. However, the probability of interface contamination is much higher for the Cu/capping layer interface, since there are vacuum interruptions and delay times associated with the manufacturing process. Void trapping in CuAl interconnects can be attributed to the passivation of the inner void surfaces with Al as shown in section 4.1.3. This finding underlines the impact of metallic impurities on the mobility of Cu atoms at interfaces.

Once a local delamination had been formed and the voids started to move and grow, several additional effects were observed during the *in-situ* SEM investigations. The interfaces were completely restored, and reasonable adhesion was regained after a void or delamination had passed through it. Furthermore, the voids experienced shape changes as they moved. Voids that moved along the Cu/capping layer interface in pure Cu interconnects usually remained shallow and did not extend vertically. Only after reaching the end of the line, the voids extended down into it. In CuAl interconnects, the voids changed their shapes as they moved along the Cu/barrier interface at the bottom of the lines. The vertical extension as well as the length of the voids varied on the way. The post-mortem EBSD investigations revealed a correlation between the shape changes and the position of grain boundaries. Since the activation energy for grain boundary diffusion is lower than that for Cu/barrier interface diffusion (compare to table 2.1), a contribution from grain boundary diffusion has to be taken into account. This explains the more pronounced vertical extension of voids in CuAl interconnects compared to Cu interconnects.

CoWP-coated Cu interconnect samples showed a similar behavior. The voids nucleated and moved on all interfaces and within the bulk of the metal lines, suggesting an even stronger contribution from the Cu microstructure. The post-mortem EBSD investigations showed slit voids in one sample and a spherical void in the line with some facets in another sample. The slit voids coincided with grain boundaries and the spherical void suggests that an entire grain was decomposed.

In conclusion, void movement along an interface cannot be explained on the basis of a moving delamination alone. Instead, material redeposition along the inner void surface has to be taken into account as well. As shown in

tables 2.1 and 2.2, the activation energies for the migration of Cu atoms along Cu surfaces are much lower than that for migration along interfaces. Consequently, there will be more atoms transported across the inner void surface than can be removed through the interface behind the void. As a result, voids have an accumulation region on the anode side and a depletion region on the cathode side. The redeposition process causes the voids to move. It is also responsible for the restoration of the interface after the void passed through it. Direct evidence for this mechanism was found during the final stages of the experiments. Significant redeposition from the bottom of the vias into the top part of it was observed frequently. Figure 5.2 illustrates the redeposition process.

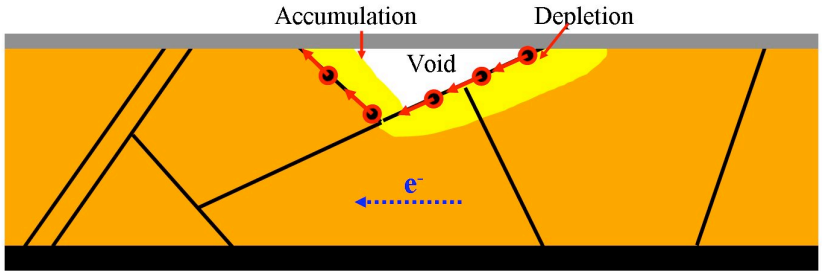


Fig. 5.2: Material redeposition across a void surface during EM.

5.2.3 Effects of Al addition on the properties of CuAl interconnects

A strong effect of the Al addition was observed on the electrical properties of the interconnects. The resistivity increased significantly by almost 42 % compared to Cu interconnects. At the same time, the temperature coefficient of resistivity was reduced by 39 %. An important aspect of the formation of CuAl interconnects is the evolution of the resistivity during wafer processing. After the first thermal treatment (Metal 5 anneal: 250 °C for 30 min.), it remained on the same level as the resistivity of pure Cu interconnects. This result means, that no significant Al diffusion from the TaAl barrier into the Cu line had occurred. After processing of three additional levels of metallization, the resistivity had increased by 42 %. The thermal budgets that the wafers experienced for each layer were similar. This observation indicates that the Al diffusion along Cu grain boundaries is a slow process. From the resistance data of the standard accelerated lifetime tests, an activation energy for the diffusion of Al from the TaAl layer into the Cu line of 1.79 eV was determined.

These observations have implications for the manufacturing processes. Since the improved EM reliability is attributed to the enrichment of Al at the Cu/capping layer interface, it is expected that the CuAl interconnects would not exhibit such an improvement if they were tested directly after processing and capping with SiN_x alone. Moreover, the continuous resistance increase that was observed during the standard accelerated lifetime test has to be expected during chip operation as well. This effect may compromise its functionality without leading to failed interconnects. It is important to note, that the Via 4 resistance was already increased after Metal 5-CMP and did not increase much further after full processing. The resistance of vias is generally dominated by the resistivity of the barrier at the bottom. This means that, as expected from an alloy barrier, the resistivity of the TaAl barrier is significantly increased.

The observation that the resistivity increase in CuAl interconnects occurred only after multiple heat treatments has additional implications for the interpretation of the differences in the atomic structure of the Cu/capping layer interface. Without significant Al incorporation into the Cu line after Metal 5-CMP, the Cu surface of the CuAl interconnects is assumed to be identical to that of pure Cu interconnects at that time. Consequently, an intermixing layer should have been formed during the subsequent deposition of the SiN_x capping layer, similar to that found in pure Cu interconnects. However, in fully processed CuAl interconnects, the intermixing layer was not present anymore. Instead, the interface appeared mostly crystalline and highly ordered. It is assumed, that the intermixing layer was dissolved during the thermal treatments of three additional metal layers, forming a compound region that contains Si and N in addition to Al.

On unstressed samples, it was found, that Al initially resided at the grain boundaries and at the Cu/capping layer interface of the metal lines. Local concentrations of up to 10 at.-% at grain boundaries and up to 4 at.-% at the Cu/capping layer interface were measured. From the Cu-Al phase diagram follows that the solid solubility of Al in Cu at room temperature is in the range of 19 at.-% [76]. Based on these results, the formation of a substitutional solid solution is expected, rather than separate intermetallic phases.

The Al addition had a significant impact on the microstructure of CuAl interconnects compared to pure Cu interconnects. CuAl interconnects showed a significantly increased Cu<111>-texture (63 % vs. 40 %). The grain size was slightly increased, and the amount of twin grains was reduced. The increase of the grain size is partly related to the reduction of twin grains. The comparison of the total length of the grain boundary network to the total length of

Σ-3 boundaries revealed, that the total length of non-Σ-3 boundaries is almost identical for Cu and CuAl interconnects. The total length of Σ-3 boundaries is significantly longer in Cu interconnects. Also, there were less clusters of small grains between bamboo-like sections of the metal lines observed in the EBSD analyses of cross-sections of the CuAl interconnects. It is known that the texture as well as the grain size of Cu interconnects are strongly influenced by the properties of the barrier material [77]. The TaAl barrier used in CuAl interconnects is significantly different to the standard Ta barrier used in pure Cu interconnect. It is likely that the differences in microstructure can be attributed to this. Furthermore, twin boundaries are highly ordered, defect-free interfaces. Their formation seems to be suppressed in CuAl interconnects due to the presence of additional impurities (Al).

Chapter 6

Conclusions

An experimental setup for *in-situ* SEM investigations of EM-induced degradation phenomena in fully embedded Cu interconnect structures was developed. Experiments can be run at temperatures up to 400 °C over extended periods of time. The full automation of the SEM imaging routine allows to study samples with very long lifetimes without user interaction. Continuous image recording is possible at short imaging intervals. A sample realignment algorithm ensures that the region of interest remains within the field-of-view of the microscope. The setup was designed to image cross-sections of multilevel interconnect structures. It is possible to observe the top Cu/capping layer interface and the bottom Cu/barrier interface of inlaid Cu interconnects simultaneously. The resulting images or video sequences provide detailed visualizations of void nucleation and evolution processes. The sample preparation routine was optimized for best possible SEM image quality, ensuring that further post-mortem analyses, such as TEM/EDS or SEM/EBSD at cross-sections of the tested samples can be performed.

The *in-situ* investigation of Cu, CuAl, and CoWP-coated interconnects revealed that the observed significant differences in EM lifetimes are connected to fundamental changes in the degradation mechanisms. In Cu interconnects, the top Cu/capping interface serves as the dominating diffusion path. Void nucleation and evolution occurs mainly at that interface. In CuAl and CoWP-coated Cu interconnects, the Cu/barrier interfaces act as the dominating material transport path instead. A significant contribution from the grain boundaries was evident for these two types of interconnects, too. Void nucleation at the Cu/capping layer interface was still observed, but did not cause the failure of the samples. The changed degradation mechanism was attributed to the introduction of metal impurities at the Cu/capping layer interface. This

interface modification leads to an increased interface strength. Another observation is that the void nucleation at the interfaces generally occurred at some distance away from the line end. Void nucleation inside the vias was never observed. This result is different to the classical understanding, that assumes the upper corner of line ends as the void nucleation site.

The microstructure of the interconnects clearly controlled the void nucleation and evolution locally. Twin grains in particular played an important role for the evolution of voids in interconnects. They exhibited a higher resistance against EM-induced decomposition than other grains and a relatively low diffusivity along the Cu/capping layer interface. A new failure mechanism was observed in CoWP-coated Cu interconnects: in some samples, slit voids were formed at grain boundaries at some distance away from the via. This mechanism depends strongly on the local configuration of the grain boundaries. It could have an impact on the standard deviation of the lognormal distribution (σ) of lifetimes. This effect reduces the extrapolated lifetimes at chip operating conditions. Microstructure engineering will be required in order to minimize this effect in interconnects with a strengthened Cu/capping layer interface. A completely bamboo-like microstructure is desirable. Alternatively, polycrystalline regions between bamboo-like segments should be shorter than the Blech length in order to reduce the contribution from grain boundary diffusion.

CuAl interconnects combine simple processing with superior EM reliability. However, the significant resistivity increase that was observed, is a major drawback for their applicability. Especially in high-performance devices, such as microprocessors, a resistance increase of the interconnects cannot be tolerated. In other applications, where long-term reliability is more important than performance, CuAl interconnects could be implemented.

In order to avoid the resistivity increase, interconnect processing has to be performed in such a way that the alloyed metal atoms are placed at the Cu/capping layer interface only. CoWP-coating of Cu interconnects addresses this issue. However, this technology involves several other drawbacks. It requires additional process steps after Cu-CMP, which makes it more expensive. Moreover, there are several performance and reliability concerns connected to this approach. Increased interline leakage due to ILD surface contamination and reduced reliability against dielectric breakdown between adjacent lines at high electric fields and temperatures are challenges to engineers in research and development and manufacturing.

Chapter 7

Outlook

This study showed that significant improvements can be achieved by incorporating metal atoms at the Cu/capping layer interface of inlaid Cu interconnect. Further research is necessary in order to develop processes that allow to localize metal atoms to the Cu/capping layer interface without degrading other properties. For CuAl interconnects or other types of Cu alloy interconnects, a threshold concentration of the alloying element has not been determined yet at which a significant gain in EM lifetime is achieved. The impact of that concentration on the resistivity of the interconnects has to be determined. Another approach would be to tailor the material combinations of alloy interconnects in such a way that the resistivity increase is counterbalanced by the reduction of TCR. As a result, the resistance of the interconnects at the chip operating temperature should match that of Cu.

This study provided evidence for the impact of local microstructure features on the EM-induced degradation of interconnects. However, it is still not completely understood, which microstructure parameter influences the overall reliability and how it can be used to improve reliability. Research is necessary in order to isolate the influence of grain size and texture of Cu interconnects from each other. Both, numerical simulation as well as carefully designed experiments could provide answers to this question. At the same time, it is necessary to develop manufacturing processes that allow to control these parameters reliably.

Another important field of work is the modeling and simulation of EM in interconnects. The models need to be able to predict the impact of interconnect properties and process parameters on the degradation mechanisms. Ultimately, they could be able to predict lifetimes and failure distributions, with the goal to reduce cost and development times.

Finally, it would be interesting to apply *in-situ* methods to other types of time-dependent phenomena, such as stress migration or temperature and bias voltage dependent dielectric breakdown. Other optical techniques, such as OBIRCH (optical beam induced resistance change) could also be used *in-situ*, especially for the observation of leakage mechanisms in interconnect structures.

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